EXHIBIT F

Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800, EP-TA845, S2MM101

Title: POWER SYSTEM WITH POWER CONVERTERS HAVING AN ADAPTIVE CONTROLLER

Priority Date: Dec. 01, 2006

Filed Date: Feb. 23, 2007

Issued Date: Mar. 09, 2010

Expiration Date: Aug 06, 2027

Inventors: Daniel A. Artusi; Ross Fosler; Allen F. Rozman

Claims: 1, 3, 6, & 16

Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800

Claim 1

A **(CON) power converter** coupled to a **(PCC) power system controller configured to receive** a **(S) signal** indicating a **(OP) system operational state** of a **(LD) load** coupled thereto, comprising:

a **(PS) power switch configured to conduct for** a **(DC) duty cycle** to provide a **(OC) regulated output characteristic** at an **(OUT) output** thereof; and

a **(CON) controller configured to receive** a **(COM) command** from said **(PCC) power system controller** to enter a **(PCOP) power converter operational state**

as a function of said **(S) signal** indicating said **(OP) system operational state**,

said **(CON) controller further configured to provide** a **(OS) signal to control** said **(DC) duty cycle** of said **(PS) power switch** as a function of said **(OC) output characteristic** and in accordance with said **(COM) command**, thereby regulating an **(IOC) internal operating characteristic** of said **(CON) power converter** to improve an operating efficiency thereof as a function of said **(OP) system operational state**.

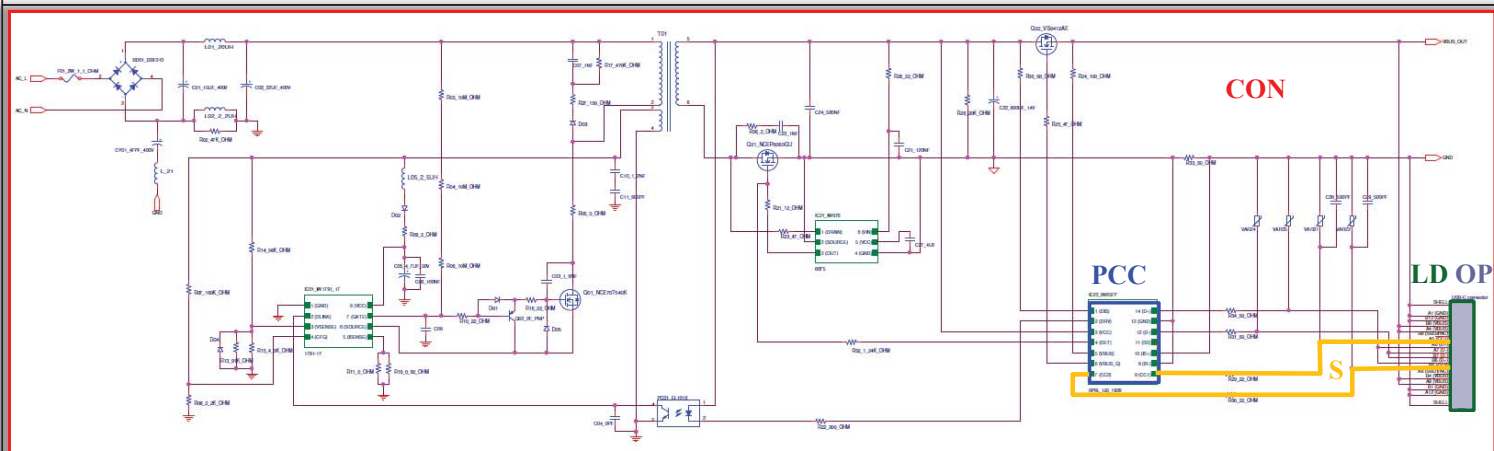| Claim 1	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800**

A **(CON) power converter** **coupled to** a **(PCC) power system controller** configured to receive a **(S) signal** indicating a **(OP) system operational state** of a **(LD) load** coupled thereto, comprising:

IC1 works in conjunction with IC21 and IC22 on the EP-TA800.

Source: Dialog Semiconductor iW657P USB Power Delivery 3.0 Controller with Integrated Current Sense Supports Qualcomm Quick Charge 4+, Product Summary Rev. 1.0 30-Mar-2020, Note: The citation pertains to only the document excerpt not the schematics or other data.

Pin Number DFN-14	Pin Name	Type	Pin Description
1	DIS	Analog Output	Discharging circuit. Used for fast discharging of output capacitor.
2	DRV	Analog Output	External circuit drive. Can be used to drive optocoupler LED with automatic current limiting for transmitting signals to primary side.
3	V_{CC}	Power Supply	IC power supply.
4	DET	Analog Input	AC unplug detect.
5	V_{BUS}	Analog Input/Output	Monitor V_{BUS} voltage after N-FET switch.
6	V_{BUS_o}	Analog Input/Output	Connect to external N-FET gate pin for gate-source voltage control.
7	CC2	Analog Input/Output	Configuration Channel 2.
8	CC1	Analog Input/Output	Configuration Channel 1.
9	IS-	Analog Input	Output current sensing terminal - (for current sensing resistor).
10	IS+	Analog Input	Output current sensing terminal + (for current sensing resistor).

Claim 1	Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800

A power converter coupled to a power system controller configured to receive a **(S) signal** indicating a **(OP) system operational state** of a load coupled thereto, comprising:

This burst of data was fed to CC1 by the external PD3.0 emulator, immediately after pressing its trigger button that sends the charger a request for 9V output at VBUS_OUT.

VBUS_OUT= 5V (no load), then transitions to 9V (no load)

Shown at 20ms/div scale in order to capture the entire transition from 5V to 9V at VBUS_OUT.

Claim 1	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800**

a **(PS) power switch configured to conduct for** a duty cycle to provide a **(OC) regulated output characteristic** at an **(OUT) output** thereof; and

4.5   Configuration Channel (CC)

4.5.1   Architectural Overview

For the USB Type-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the Source-to-Sink connection. When the device is connected through a hub, the connection between a Sink (UFP) on the hub and the Source (host port) and the connection between the Sink (device port) and a Source (DFP on the hub), are treated as separate connections. Functionally, the configuration channel is used to serve the following purposes.

- Detect attach of USB ports, e.g. a Source to a Sink
- Resolve cable orientation and twist connections to establish USB data bus routing
- Establish data roles between two attached ports
- Discover and configure VBUS: USB Type-C Current modes or *USB Power Delivery*

Source: https://usb.org/sites/default/files/USB%20Type-C%20Spec%20R2.0%20-%20August%202019.pdf, Note: The citation pertains to only the document excerpt not the schematics or other data.

Claim 1	Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800

a power switch configured to conduct for a **(DC) duty cycle** to provide a **(OC) regulated output characteristic** at an output thereof; and

Claim 1	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800**

a power switch configured to conduct for a **(DC) duty cycle** to provide a **(OC) regulated output characteristic** at an output thereof; and

OC

VBUS_OUT= 5V, no load

VBUS_OUT= 5V, 1A load **OC**

VBUS_OUT= 5V, ~3.6A load **OC**

Note: The charger will hold up the VBUS_OUT voltage at ~4.5V under a 3.5A load but the charger shuts down when the load is increased beyond that. This O-scope capture was taken as the charger was going into one of those over-current protection shutdowns when the load was increased to ~3.6A. Immediately after this capture, the VBUS_OUT voltage drops to 0V.

Claim 1	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800**

a **(CON) controller configured to receive** a **(COM) command** from said **(PCC) power system controller** to enter a **(PCOP) power converter operational state**

COM　　　　　　　**PCOP**

Pin Number	Pin Name	Type	Pin Description
1	GND	Ground	Ground.
2	DLNK	Analog Input	Digital communication link signal. Used for secondary-side to primary-side communication for all rapid change information, which includes output voltage requests, output current limits, output voltage undershoot, and over-voltage protection.
3	V_{SENSE}	Analog Input	Auxiliary voltage sense. Used for primary-side regulation and secondary-to-primary communication through main transformer.
4	CFG	Analog Input	Used for CDC configuration and auxiliary winding open protection.
5	I_{SENSE}	Analog Input	Primary-side current sense. Used for cycle-by-cycle peak-current control and limit in primary-side CV/CC regulation.
6	SOURCE	Power Input	Connect to the source of external power MOSFET. Inside the IC, it is connected to internal MOSFET and startup V_{CC} charge circuit.
7	GATE	Output	Gate drive for external MOSFET switch.
8	V_{CC}	Power Input	IC power supply.

Source: Dialog Semiconductor iW1791 AC/DC Primary Side Rapid Charge PWM Controller with High Resolution Voltage/Current Control, Product Summary Rev. 1.51 05-OCT-2018, Note: The citation pertains to only the document excerpt not the schematics or other data.

| Claim 1 | | **Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800** |

as a function of said **(S) signal** indicating said **(OP) system operational state**,
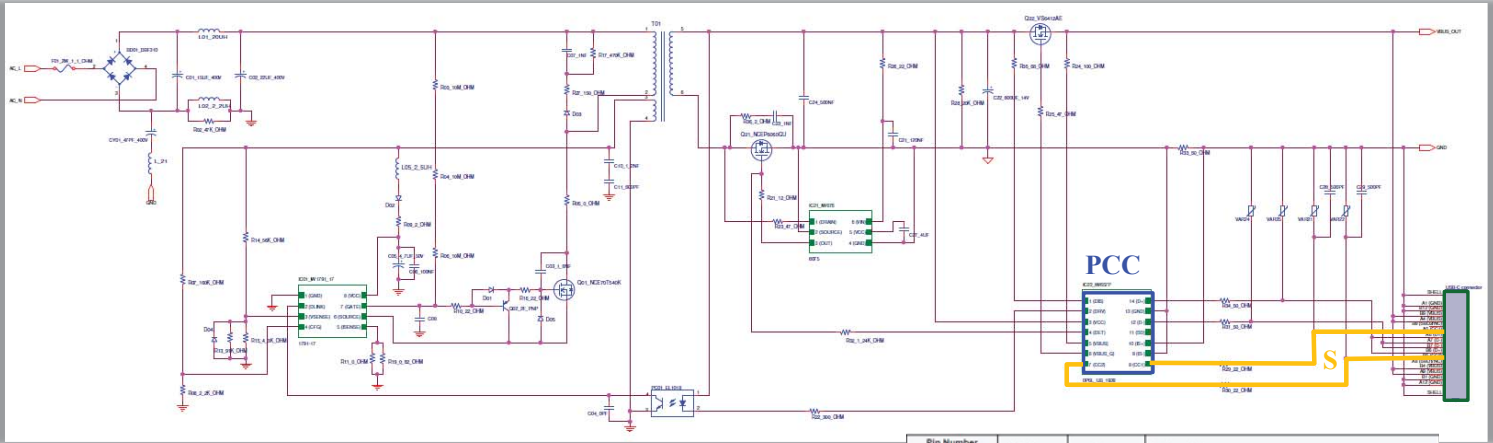
IC1 works in conjunction with
IC21 and IC22 on the EP-TA800.

Pin Number DFN-14	Pin Name	Type	Pin Description
1	DIS	Analog Output	Discharging circuit. Used for fast discharging of output capacitor.
2	DRV	Analog Output	External circuit drive. Can be used to drive optocoupler LED with automatic current limiting for transmitting signals to primary side.
3	V_{CC}	Power Supply	IC power supply.
4	DET	Analog Input	AC unplug detect.
5	V_{BUS}	Analog Input/Output	Monitor V_{BUS} voltage after N-FET switch.
6	V_{BUS_G}	Analog Input/Output	Connect to external N-FET gate pin for gate-source voltage control.
7	CC2	Analog Input/Output	Configuration Channel 2.
8	CC1	Analog Input/Output	Configuration Channel 1.
9	IS-	Analog Input	Output current sensing terminal - (for current sensing resistor).
10	IS+	Analog Input	Output current sensing terminal + (for current sensing resistor).
11	SD	Analog Input/Output	Connect to an external NTC resistor to measure the power adapter temperature.
12	D-	Analog Input/Output	USB D- signal.
13	GND	Ground	Ground.
14	D+	Analog Input/Output	USB D+ signal.

Source: Dialog Semiconductor iW657P USB Power Delivery 3.0 Controller with Integrated Current Sense Supports Qualcomm Quick Charge 4+, Product Summary Rev. 1.0 30-Mar-2020, Note: The citation pertains to only the document excerpt not the schematics or other data.

Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800

Claim 1

as a function of said **(S) signal** indicating said **(OP) system operational state**,

Source: Dialog Semiconductor iW1791 AC/DC Primary Side Rapid Charge PWM Controller with High Resolution Voltage/Current Control, Product Summary Rev. 1.51 05-OCT-2018, Note: The citation pertains to only the document excerpt not the schematics or other data.

Claim 1	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800**

said **(CON) controller further configured to provide** a **(OS) signal to control** said duty cycle of said **(PS) power switch** as a function of said output characteristic and in accordance with said **(COM) command,**

Pin Number	Pin Name	Type	Pin Description
1	GND	Ground	Ground.
2	DLNK	Analog Input	Digital communication link signal. Used for secondary-side to primary-side communication for all rapid change information, which includes output voltage requests, output current limits, output voltage undershoot, and over-voltage protection.
3	V_{SENSE}	Analog Input	Auxiliary voltage sense. Used for primary-side regulation and secondary-to-primary communication through main transformer.
4	CFG	Analog Input	Used for CDC configuration and auxiliary winding open protection.
5	I_{SENSE}	Analog Input	Primary-side current sense. Used for cycle-by-cycle peak-current control and limit in primary-side CV/CC regulation.
6	SOURCE	Power Input	Connect to the source of external power MOSFET. Inside the IC, it is connected to internal MOSFET and startup V_{CC} charge circuit.
7	GATE	Output	Gate drive for external MOSFET switch.
8	V_{CC}	Power Input	IC power supply.

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Claim 1	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800**

said controller further configured to provide a signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said **(COM) command,**

Programming data burst from external PD3.0 emulator sent to Pin 8 (CC1) of IC22 (iW657P)

Programming data burst from Pin 2 (DRV) of IC22 sent to photocouple (PC01) for transmission to Pin 2 (DLINK) of IC01 (iW1791) in the primary side.

Gate of Q01

CC1

COM Pin 2 (DRV)

VBUS_OUT

Trigger button pressed

IC22 (iW657P) has decoded external PD3.0 commands and now begins internal "DLINK" transmission to IC01(iW1791) in the primary side.
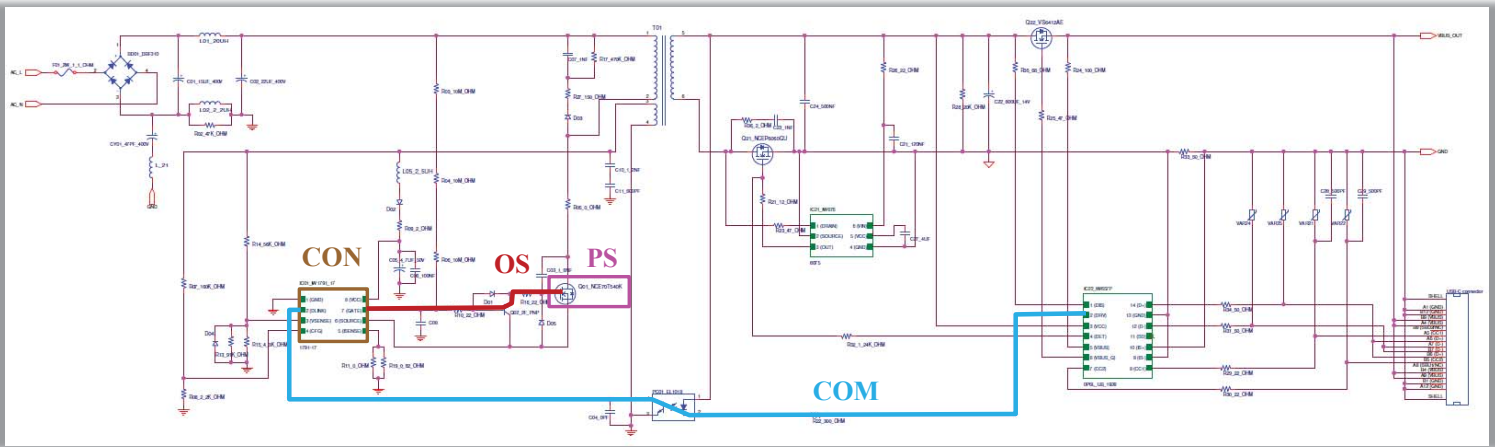
VBUS_OUT completes 5V to 9V transition

COM

Pin Number	Pin Name	Type	Pin Description
1	GND	Ground	Ground.
2	DLNK	Analog Input	Digital communication link signal. Used for secondary-side to primary-side communication for all rapid change information, which includes output voltage requests, output current limits, output voltage undershoot, and over-voltage protection.
3	V_{SENSE}	Analog Input	Auxiliary voltage sense. Used for primary-side regulation and secondary-to-primary communication through main transformer.
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7	GATE	Output	Gate drive for external MOSFET switch.
8	V_{CC}	Power Input	IC power supply.

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Preliminary – Subject to Change

12

Claim 1	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800**

said controller further configured to provide a signal to control said **(DC) duty cycle** of said power switch as a function of said **(OC) output characteristic** and in accordance with said command,

Claim 1	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800**

said controller further configured to provide a signal to control said **(DC) duty cycle** of said power switch as a function of said **(OC) output characteristic** and in accordance with said command,
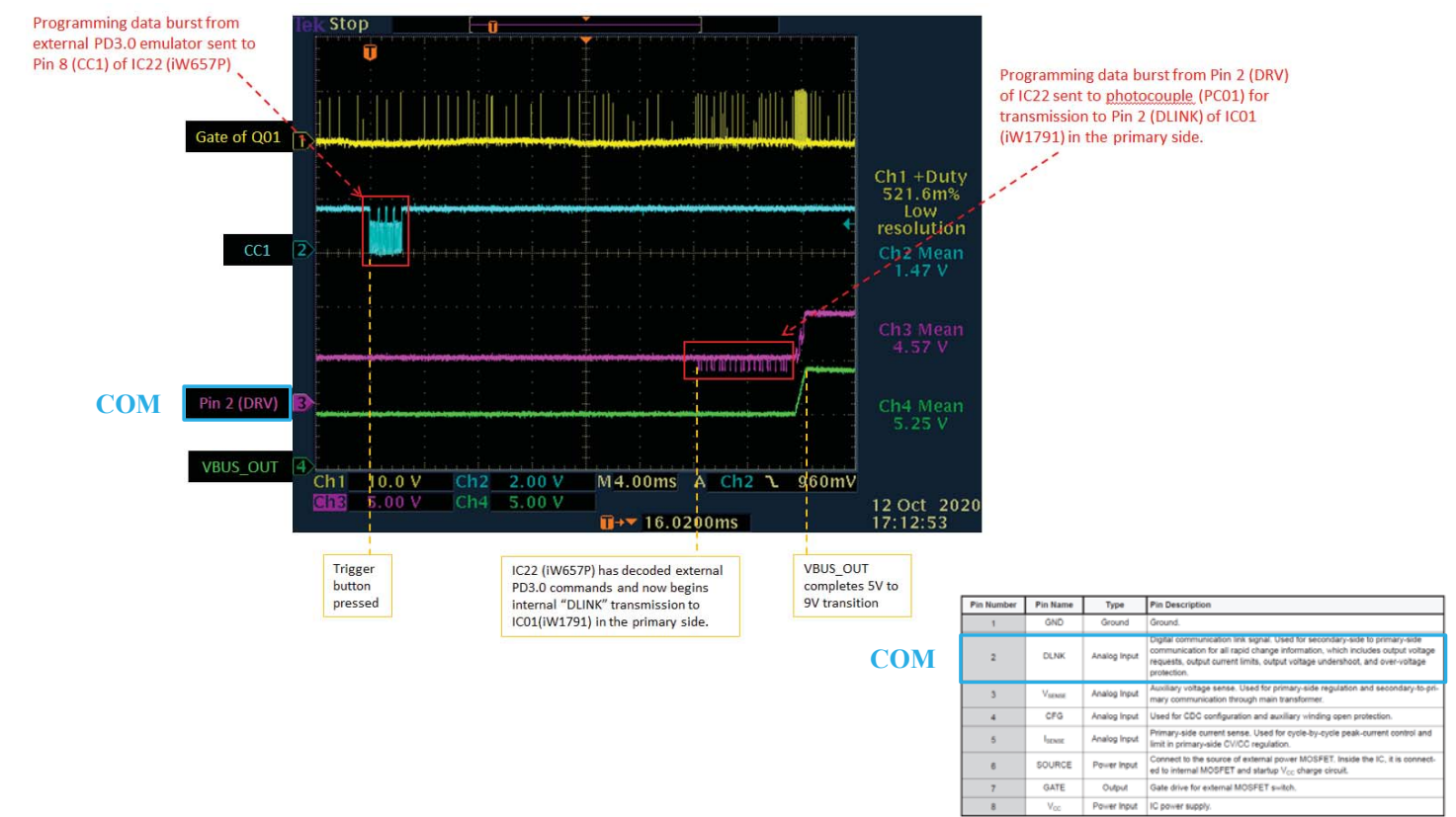

OC
VBUS_OUT= 5V, no load

VBUS_OUT= 5V, 1A load OC

VBUS_OUT= 5V, ~3.6A load   OC

Note: The charger will hold up the VBUS_OUT voltage at ~4.5V under a 3.5A load but the charger shuts down when the load is increased beyond that. This O-scope capture was taken as the charger was going into one of those over-current protection shutdowns when the load was increased to ~3.6A. Immediately after this capture, the VBUS_OUT voltage drops to 0V.

Claim 1	Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800

thereby regulating an **(IOC) internal operating characteristic** of said **(CON) power converter** to improve an operating efficiency thereof as a function of said **(OP) system operational state**.

CON

iW1791

AC/DC Primary-Side Rapid Charge™ PWM Controller
with High Resolution Voltage/Current Control

OP

Dialog's innovative proprietary technology ensures that power supplies designed with the iW1791 and Dialog's secondary-side controllers can provide output voltage configurations of 3V to 20V for USB PD, 5V/9V/12V for QC2.0 and 3.6V to 12V in 200mV increments for QC3.0 and other proprietary protocols.

IOC

- Proprietary optimized load adaptive maximum constant frequency PWM switching with quasi-resonant operation achieves best size, efficiency, and common mode noise
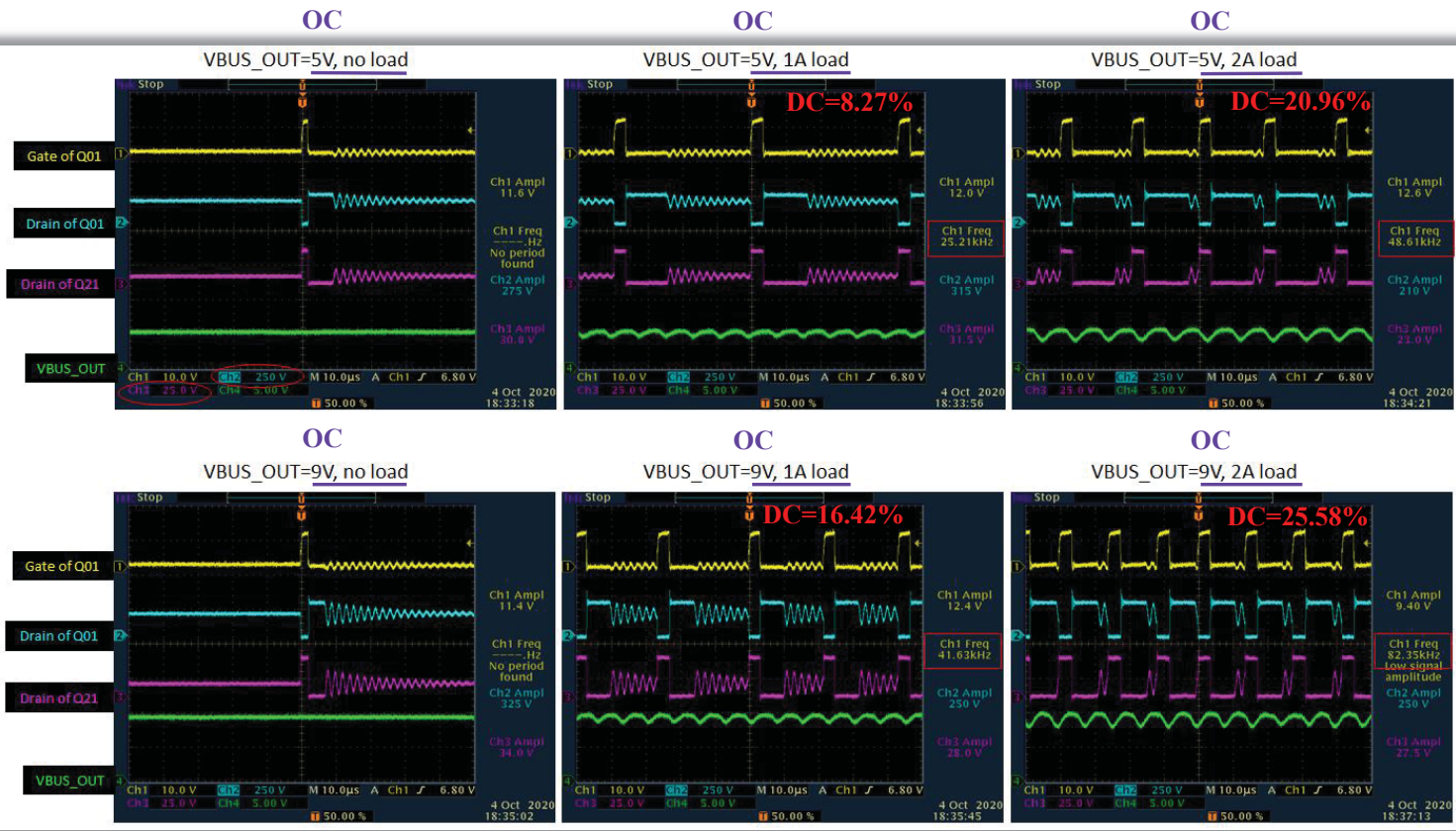
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Claim 1	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800**

thereby regulating an internal operating characteristic of said power converter to **(EFF) improve an operating efficiency** thereof as a function of said **(OP) system operational state**.

<div align="center">

OP   **EFF**

</div>

EP-TA800 (5V testing)

vin	I_in (A)	meas_W_in	V_out	I_out (A)	calc_W_out	meas_W_out	Efficiency
	0.008	0.000	5.120	0.000	0.000	0.000	
	0.011	0.412	5.110	0.020	0.102	0.148	0.359
	0.021	0.800	5.100	0.100	0.510	0.522	0.653
	0.062	2.990	5.080	0.500	2.540	2.595	0.868
	0.101	5.550	5.070	1.000	5.070	5.109	0.921
	0.148	8.635	5.020	1.500	7.530	7.542	0.873
	0.185	11.240	5.000	2.000	10.000	9.983	0.888
	0.222	14.130	4.980	2.500	12.450	12.560	0.889

EP-TA800 (9V testing)

vin	I_in (A)	meas_W_in	V_out	I_out (A)	calc_W_out	meas_W_out	Efficiency
	0.015	0.554	9.140	0.000	0.000	0.000	
	0.022	0.858	9.130	0.020	0.183	0.266	0.310
	0.035	1.521	9.130	0.100	0.913	0.933	0.613
	0.099	5.399	9.100	0.500	4.550	4.650	0.861
	0.171	10.210	9.090	1.000	9.090	9.152	0.896
	0.241	15.230	9.080	1.500	13.620	13.640	0.896
	0.305	19.670	9.000	2.000	18.000	18.060	0.918
	0.375	24.830	8.990	2.500	22.475	22.680	0.913
	0.437	30.450	8.970	3.000	26.910	27.035	0.888

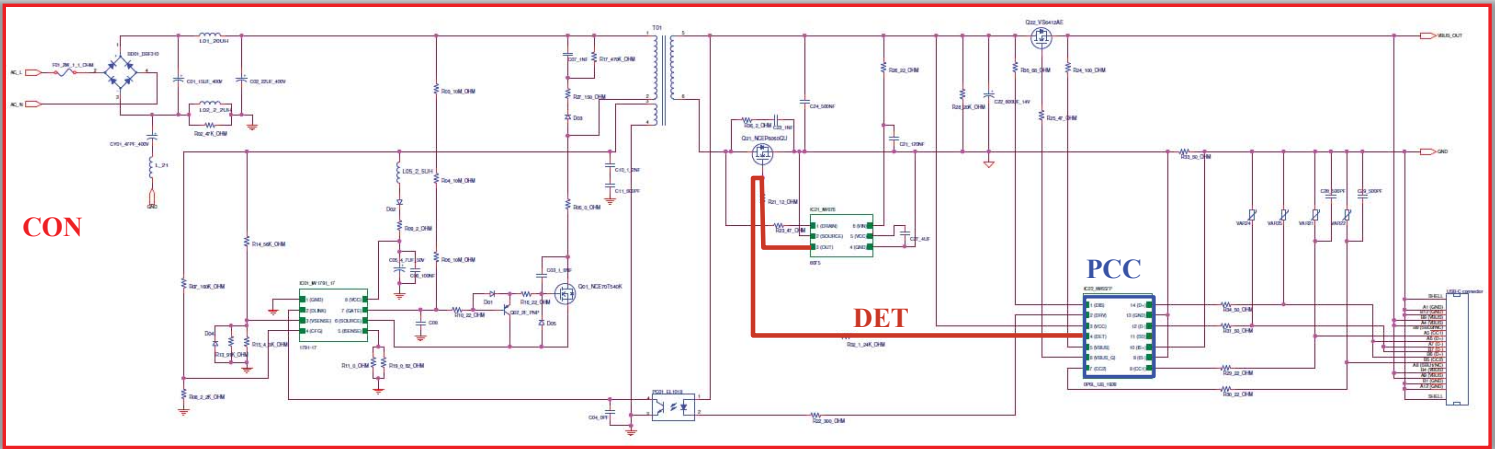**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800**

Claim 3

The power converter as recited in claim 1 wherein said **(PCC) power system controller** is configured to receive a **(DET) signal** indicating a **(STAT) power converter status** of said **(CON) power converter**,

said **(PCOP) power converter operational state** being a function of said **(STAT) power converter status**.

| Claim 3 | **Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800** |

The power converter as recited in claim 1 wherein said **(PCC) power system controller** is configured to receive a **(DET) signal** indicating a **(STAT) power converter status** of said **(CON) power converter**,

Pin Number DFN-14	Pin Name	Type	Pin Description
1	DIS	Analog Output	Discharging circuit. Used for fast discharging of output capacitor.
2	DRV	Analog Output	External circuit drive. Can be used to drive optocoupler LED with automatic current limiting for transmitting signals to primary side.
3	V_{CC}	Power Supply	IC power supply.
4	DET	Analog Input	AC unplug detect.
5	V_{BUS}	Analog Input/Output	Monitor V_{BUS} voltage after N-FET switch.
6	V_{BUS_G}	Analog Input/Output	Connect to external N-FET gate pin for gate-source voltage control.
7	CC2	Analog Input/Output	Configuration Channel 2.
8	CC1	Analog Input/Output	Configuration Channel 1.
9	IS-	Analog Input	Output current sensing terminal - (for current sensing resistor).
10	IS+	Analog Input	Output current sensing terminal + (for current sensing resistor).

Source: Dialog Semiconductor iW657P USB Power Delivery 3.0 Controller with Integrated Current Sense Supports Qualcomm Quick Charge 4+, Product Summary Rev. 1.0

Preliminary – Subject to Change

18

| Claim 3 | **Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800** |

said **(PCOP) power converter operational state** being a function of said **(STAT) power converter status**.

Pin Number DFN-14	Pin Name	Type	Pin Description	
1	DIS	Analog Output	Discharging circuit. Used for fast discharging of output capacitor.	
2	DRV	Analog Output	External circuit drive. Can be used to drive optocoupler LED with automatic current limiting for transmitting signals to primary side.	
3	V_{CC}	Power Supply	IC power supply.	
4	DET	Analog Input	AC unplug detect.	**STAT / PCOP**
5	V_{BUS}	Analog Input/ Output	Monitor V_{BUS} voltage after N-FET switch.	
6	V_{BUS_G}	Analog Input/ Output	Connect to external N-FET gate pin for gate-source voltage control.	
7	CC2	Analog Input/ Output	Configuration Channel 2.	
8	CC1	Analog Input/ Output	Configuration Channel 1.	
9	IS-	Analog Input	Output current sensing terminal - (for current sensing resistor).	
10	IS+	Analog Input	Output current sensing terminal + (for current sensing resistor).	

Note: If an AC unplug detect is observed the **(PCOP) of the system is unpowered**.

Source: Dialog Semiconductor iW657P USB Power Delivery 3.0 Controller with Integrated Current Sense Supports Qualcomm Quick Charge 4+, Product Summary Rev. 1.0 30-Mar-2020

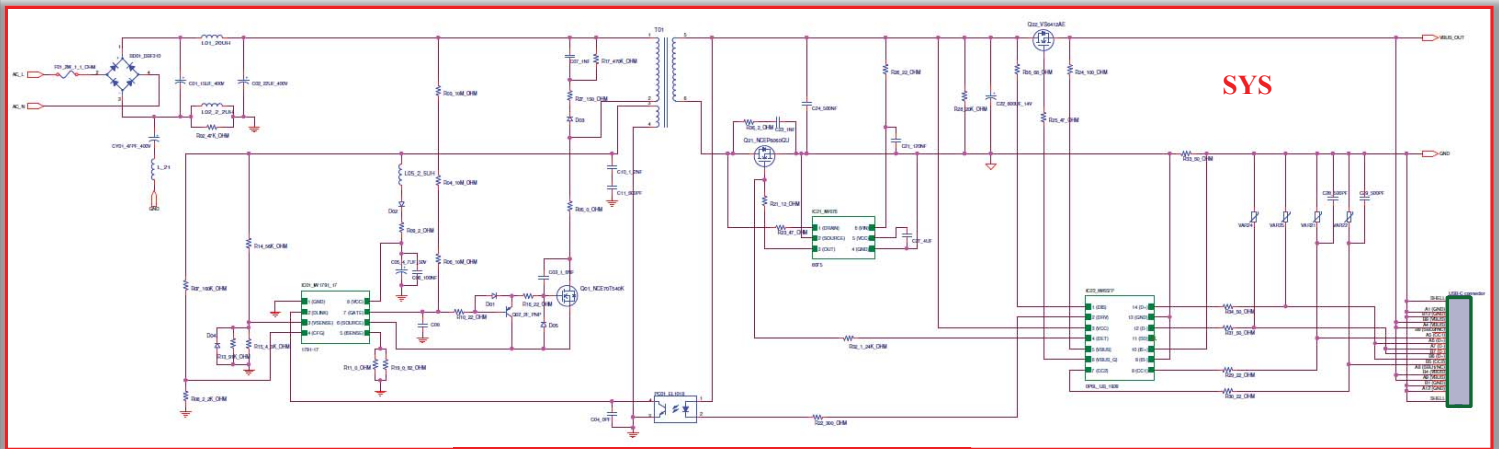**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800**

Claim 6

A **(SYS) power system** coupled to a **(LD) load**, comprising:

a **(PCC) power system controller configured to receive** a **(S) signal** indicating a **(OP) system operational state** of said **(LD) load** and

to select a **(PCOP) power converter operational state** as a function thereof; and

a **(CON) power converter**, including:

a **(PS) power switch configured to conduct for** a **(DC) duty cycle** to provide a **(OC) regulated output characteristic** at an **(OUT) output** thereof, and

a **(CON) controller configured to receive** a **(COM) command** from said **(PCC) power system controller** to enter said **(PCOP) power converter operational state** and

to provide a **(S) signal to control** said **(DC) duty cycle** of said **(PS) power switch** as a function of said **(OC) output characteristic** and in accordance with said **(COM) command**,

thereby regulating an **(IOC) internal operating characteristic** of said **(CON) power converter** to **(EFF) improve an operating efficiency thereof** as a function of said **(OP) system operational state**.

| Claim 6 | **Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800** |

A **(SYS) power system** **coupled to** a **(LD) load**, comprising:

IC1 works in conjunction with
IC21 and IC22 on the EP-TA800.

Source: Dialog Semiconductor iW657P USB
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2020, Note: The citation pertains to only the
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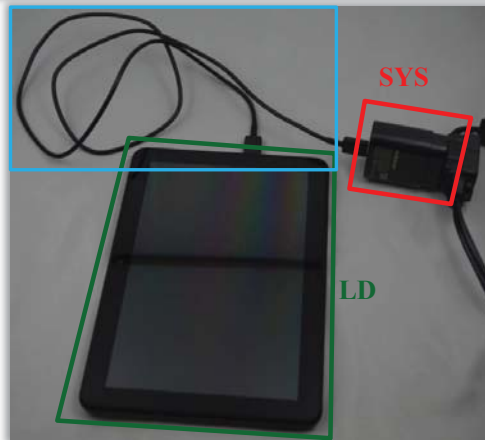
Claim 6	Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800

a **(PCC)** **power system controller configured to receive** a **(S) signal** indicating a **(OP) system operational state** of said **(LD) load** and

IC1 works in conjunction with IC21 and IC22 on the EP-TA800.

Source: Dialog Semiconductor iW657P USB Power Delivery 3.0 Controller with Integrated Current Sense Supports Qualcomm Quick Charge 4+, Product Summary Rev. 1.0 30-Mar-2020, Note: The citation pertains to only the document excerpt not the schematics or other data.
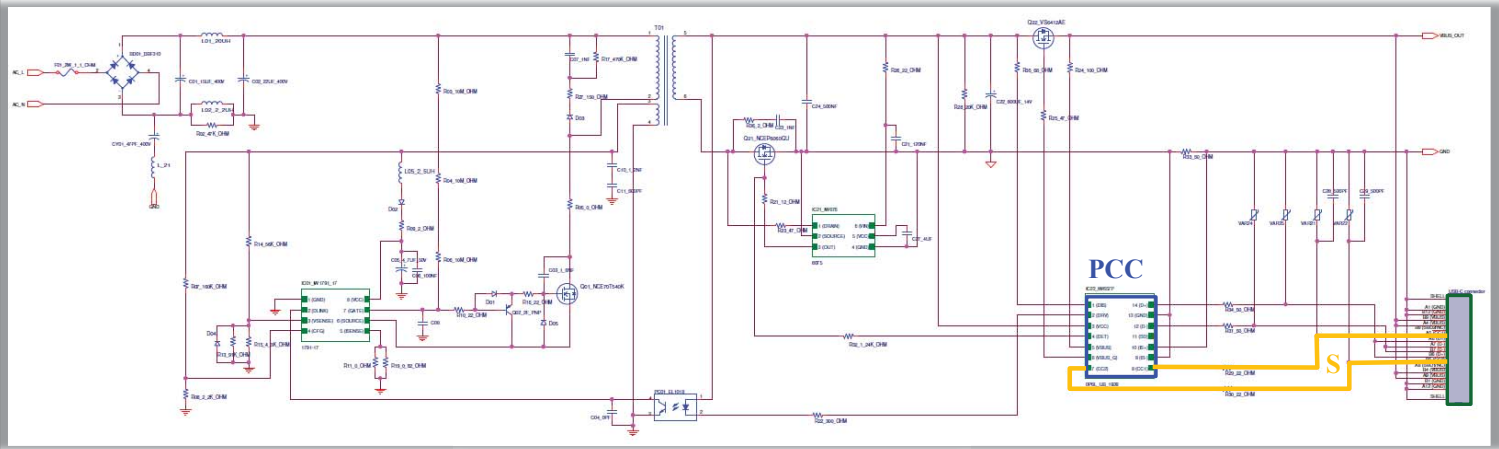
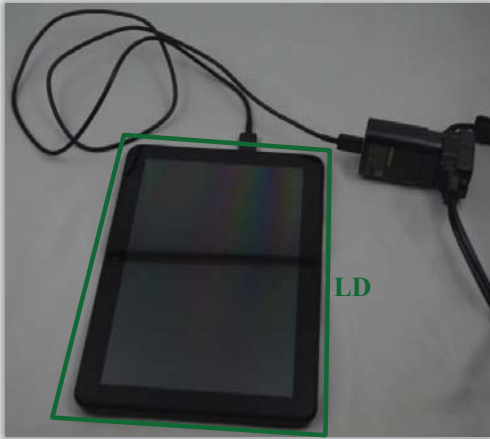| Pin Number DFN-14	Pin Name	Type	Pin Description
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3	V_CC	Power Supply	IC power supply.
4	DET	Analog Input	AC unplug detect.
5	V_BUS	Analog Input/Output	Monitor V_BUS voltage after N-FET switch.
6	V_BUS_O	Analog Input/Output	Connect to external N-FET gate pin for gate-source voltage control.
7	CC2	Analog Input/Output	Configuration Channel 2.
8	CC1	Analog Input/Output	Configuration Channel 1.
9	IS-	Analog Input	Output current sensing terminal - (for current sensing resistor).
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| Claim 6 | **Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800** |

a power system controller configured to receive a **(S) signal** indicating a **(OP) system operational state** of said load and
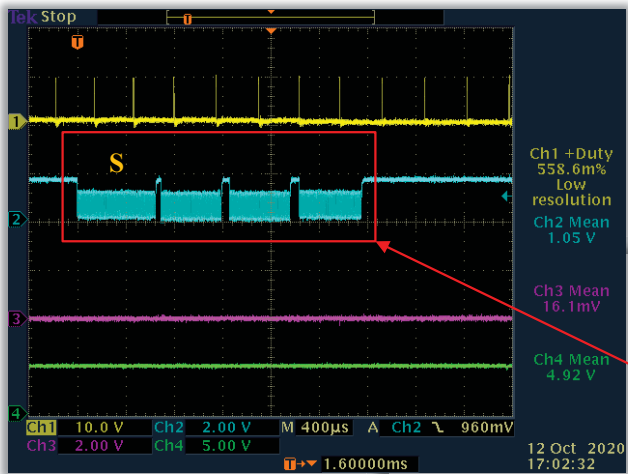
Claim 6	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800**

to select a **(PCOP) power converter operational state** as a function thereof; and

PCOP

Pin Number	Pin Name	Type	Pin Description
1	GND	Ground	Ground.
2	DLNK	Analog Input	Digital communication link signal. Used for secondary-side to primary-side communication for all rapid change information, which includes output voltage requests, output current limits, output voltage undershoot, and over-voltage protection.
3	V_{SENSE}	Analog Input	Auxiliary voltage sense. Used for primary-side regulation and secondary-to-primary communication through main transformer.
4	CFG	Analog Input	Used for CDC configuration and auxiliary winding open protection.
5	I_{SENSE}	Analog Input	Primary-side current sense. Used for cycle-by-cycle peak-current control and limit in primary-side CV/CC regulation.
6	SOURCE	Power Input	Connect to the source of external power MOSFET. Inside the IC, it is connected to internal MOSFET and startup V_{CC} charge circuit.
7	GATE	Output	Gate drive for external MOSFET switch.
8	V_{CC}	Power Input	IC power supply.

Source: Dialog Semiconductor iW1791 AC/DC Primary Side Rapid Charge PWM Controller with High Resolution Voltage/Current Control, Product Summary Rev. 1.51 05-OCT-2018, Note: The citation pertains to only the document excerpt not the schematics or other data.

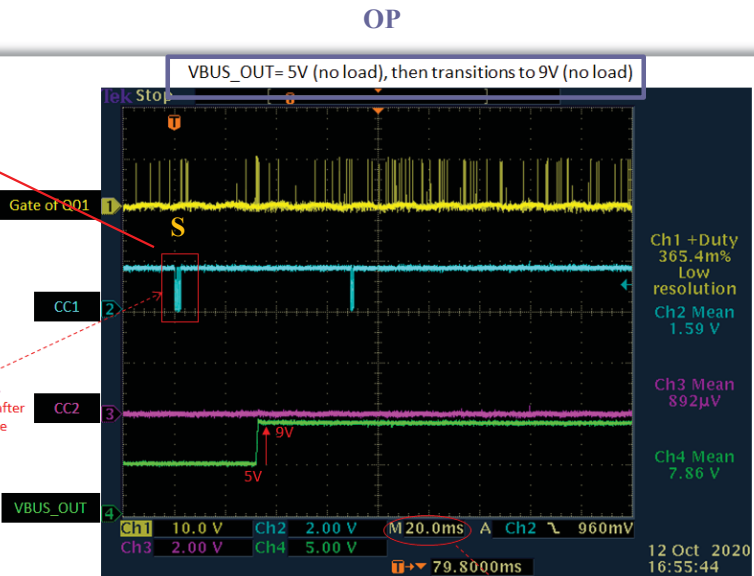| Claim 6	Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800

a **(CON) power converter**, including:

IC1 works in conjunction with
IC21 and IC22 on the EP-TA800.

Claim 6	Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800

a **(PS) power switch configured to conduct for** a duty cycle to provide a **(OC) regulated output characteristic** at an **(OUT) output** thereof, and

4.5   Configuration Channel (CC)

4.5.1   Architectural Overview

For the USB Type-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the Source-to-Sink connection. When the device is connected through a hub, the connection between a Sink (UFP) on the hub and the Source (host port) and the connection between the Sink (device port) and a Source (DFP on the hub), are treated as separate connections. Functionally, the configuration channel is used to serve the following purposes.

- Detect attach of USB ports, e.g. a Source to a Sink
- Resolve cable orientation and twist connections to establish USB data bus routing
- Establish data roles between two attached ports
- Discover and configure VBUS: USB Type-C Current modes or *USB Power Delivery*

Source: https://usb.org/sites/default/files/USB%20Type-C%20Spec%20R2.0%20-%20August%202019.pdf, Note: The citation pertains to only the document excerpt not the schematics or other data.

Claim 6	Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800

a power switch configured to conduct for a **(DC) duty cycle** to provide a **(OC) regulated output characteristic** at an output thereof; and

Claim 6	Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800

a power switch configured to conduct for a **(DC) duty cycle** to provide a **(OC) regulated output characteristic** at an output thereof, and
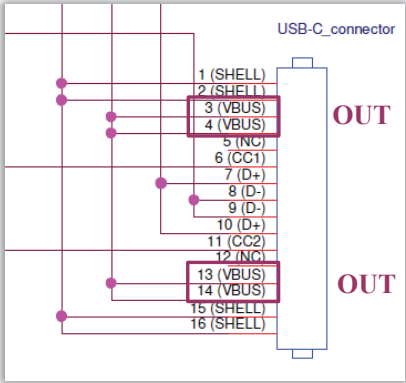

Note: The charger will hold up the VBUS_OUT voltage at ~4.5V under a 3.5A load but the charger shuts down when the load is increased beyond that. This O-scope capture was taken as the charger was going into one of those over-current protection shutdowns when the load was increased to ~3.6A. Immediately after this capture, the VBUS_OUT voltage drops to 0V.

| Claim 6 | **Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800** |

a **(CON) controller configured to receive** a **(COM) command** from said **(PCC) power system controller** to enter said **(PCOP) power converter operational state** and

COM   **PCOP**

Pin Number	Pin Name	Type	Pin Description
1	GND	Ground	Ground.
2	DLNK	Analog Input	Digital communication link signal. Used for secondary-side to primary-side communication for all rapid change information, which includes output voltage requests, output current limits, output voltage undershoot, and over-voltage protection.
3	V$_{SENSE}$	Analog Input	Auxiliary voltage sense. Used for primary-side regulation and secondary-to-primary communication through main transformer.
4	CFG	Analog Input	Used for CDC configuration and auxiliary winding open protection.
5	I$_{SENSE}$	Analog Input	Primary-side current sense. Used for cycle-by-cycle peak-current control and limit in primary-side CV/CC regulation.
6	SOURCE	Power Input	Connect to the source of external power MOSFET. Inside the IC, it is connected to internal MOSFET and startup V$_{CC}$ charge circuit.
7	GATE	Output	Gate drive for external MOSFET switch.
8	V$_{CC}$	Power Input	IC power supply.

Source: Dialog Semiconductor iW1791 AC/DC Primary Side Rapid Charge PWM Controller with High Resolution Voltage/Current Control, Product Summary Rev. 1.51 05-OCT-2018, Note: The citation pertains to only the document excerpt not the schematics or other data.

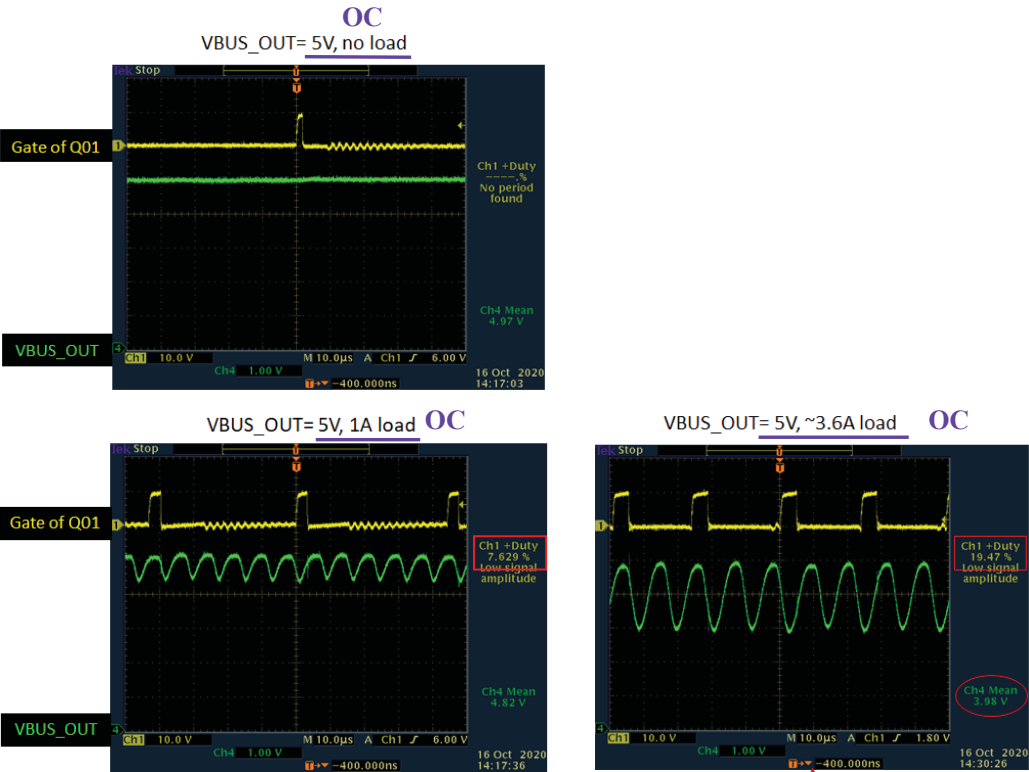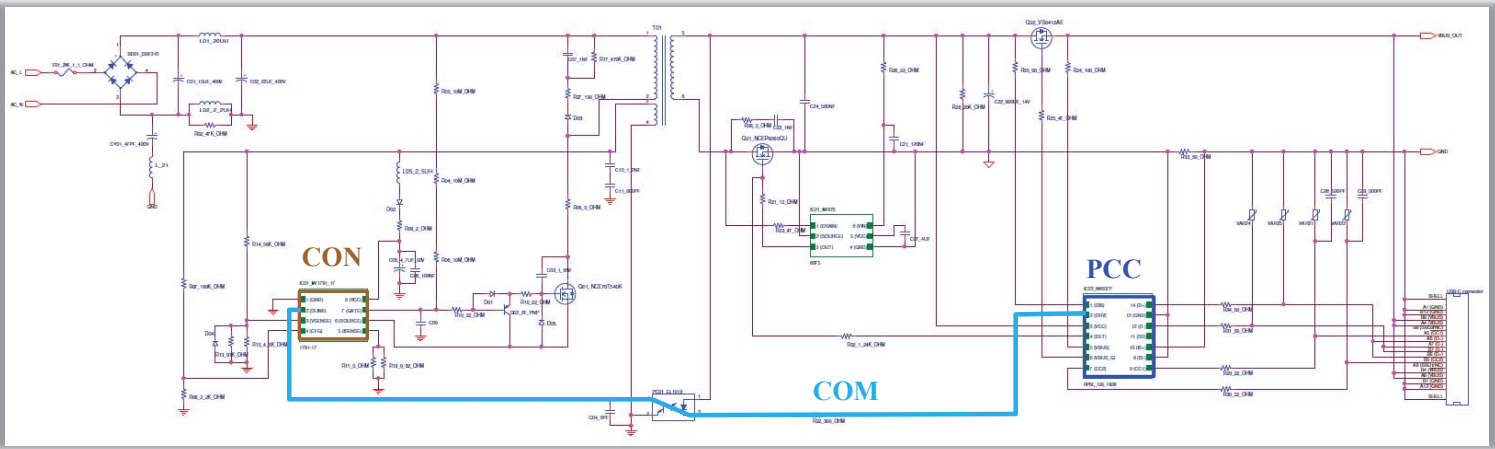| Claim 6	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800**

to provide a **(OS) signal to control** said duty cycle of said **(PS) power switch** as a function of said output characteristic and in accordance with said **(COM) command**,

Pin Number	Pin Name	Type	Pin Description
1	GND	Ground	Ground.
2	DLNK	Analog Input	Digital communication link signal. Used for secondary-side to primary-side communication for all rapid change information, which includes output voltage requests, output current limits, output voltage undershoot, and over-voltage protection.
3	V$_{SENSE}$	Analog Input	Auxiliary voltage sense. Used for primary-side regulation and secondary-to-primary communication through main transformer.
4	CFG	Analog Input	Used for CDC configuration and auxiliary winding open protection.
5	I$_{SENSE}$	Analog Input	Primary-side current sense. Used for cycle-by-cycle peak-current control and limit in primary-side CV/CC regulation.
6	SOURCE	Power Input	Connect to the source of external power MOSFET. Inside the IC, it is connected to internal MOSFET and startup V$_{CC}$ charge circuit.
7	GATE	Output	Gate drive for external MOSFET switch.
8	V$_{CC}$	Power Input	IC power supply.

Source: Dialog Semiconductor iW1791 AC/DC Primary Side Rapid Charge PWM Controller with High Resolution Voltage/Current Control, Product Summary Rev. 1.51 05-OCT-2018, Note: The citation pertains to only the document excerpt not the schematics or other data.

Claim 6	Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800

to provide a signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said **(COM) command**,

Programming data burst from external PD3.0 emulator sent to Pin 8 (CC1) of IC22 (iW657P)

Programming data burst from Pin 2 (DRV) of IC22 sent to photocouple (PC01) for transmission to Pin 2 (DLINK) of IC01 (iW1791) in the primary side.

Gate of Q01

CC1

COM Pin 2 (DRV)

VBUS_OUT

Ch1 +Duty 521.6m% Low resolution

Ch2 Mean 1.47 V

Ch3 Mean 4.57 V

Ch4 Mean 5.25 V

Trigger button pressed

IC22 (iW657P) has decoded external PD3.0 commands and now begins internal "DLINK" transmission to IC01(iW1791) in the primary side.

VBUS_OUT completes 5V to 9V transition

COM

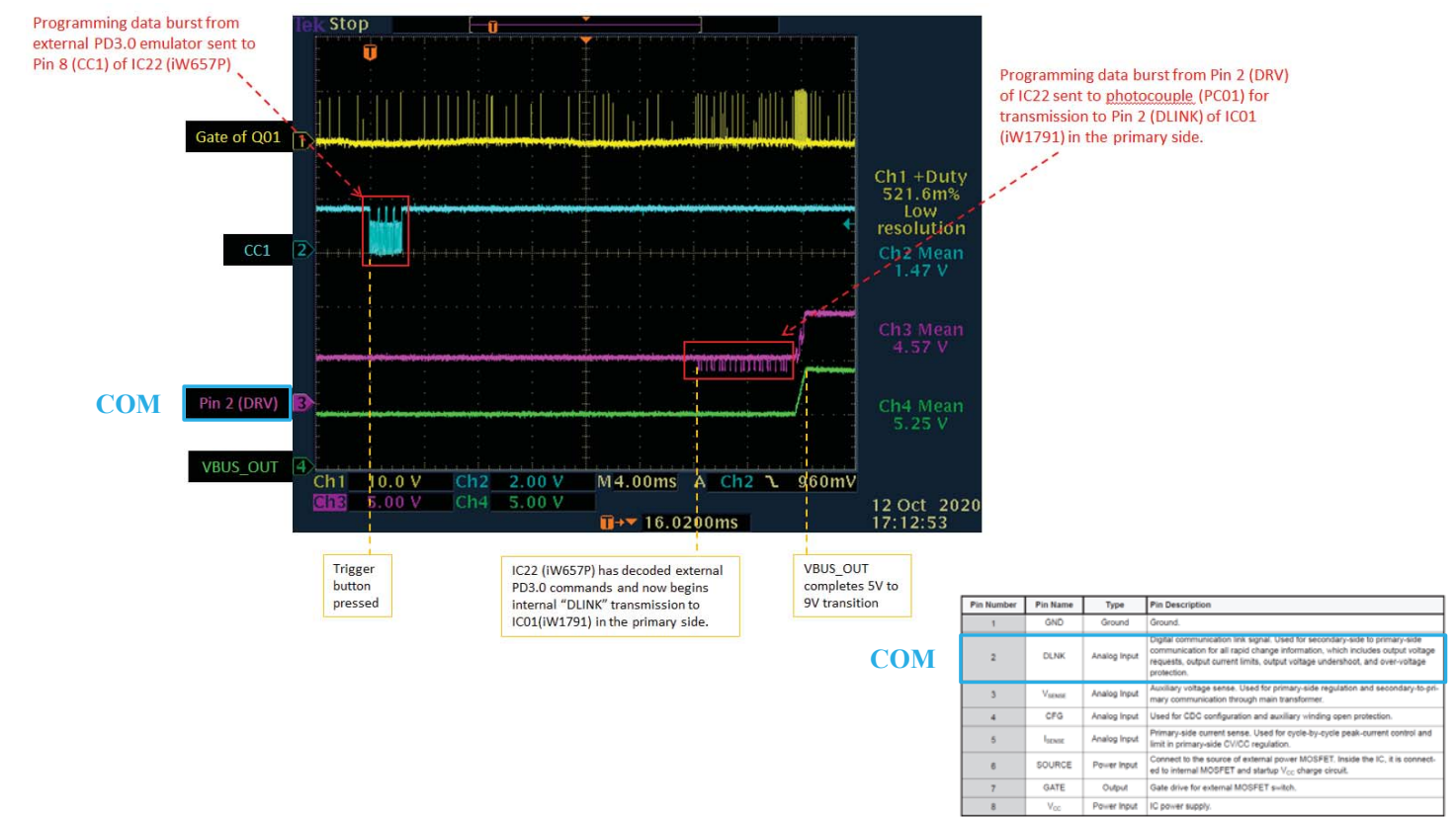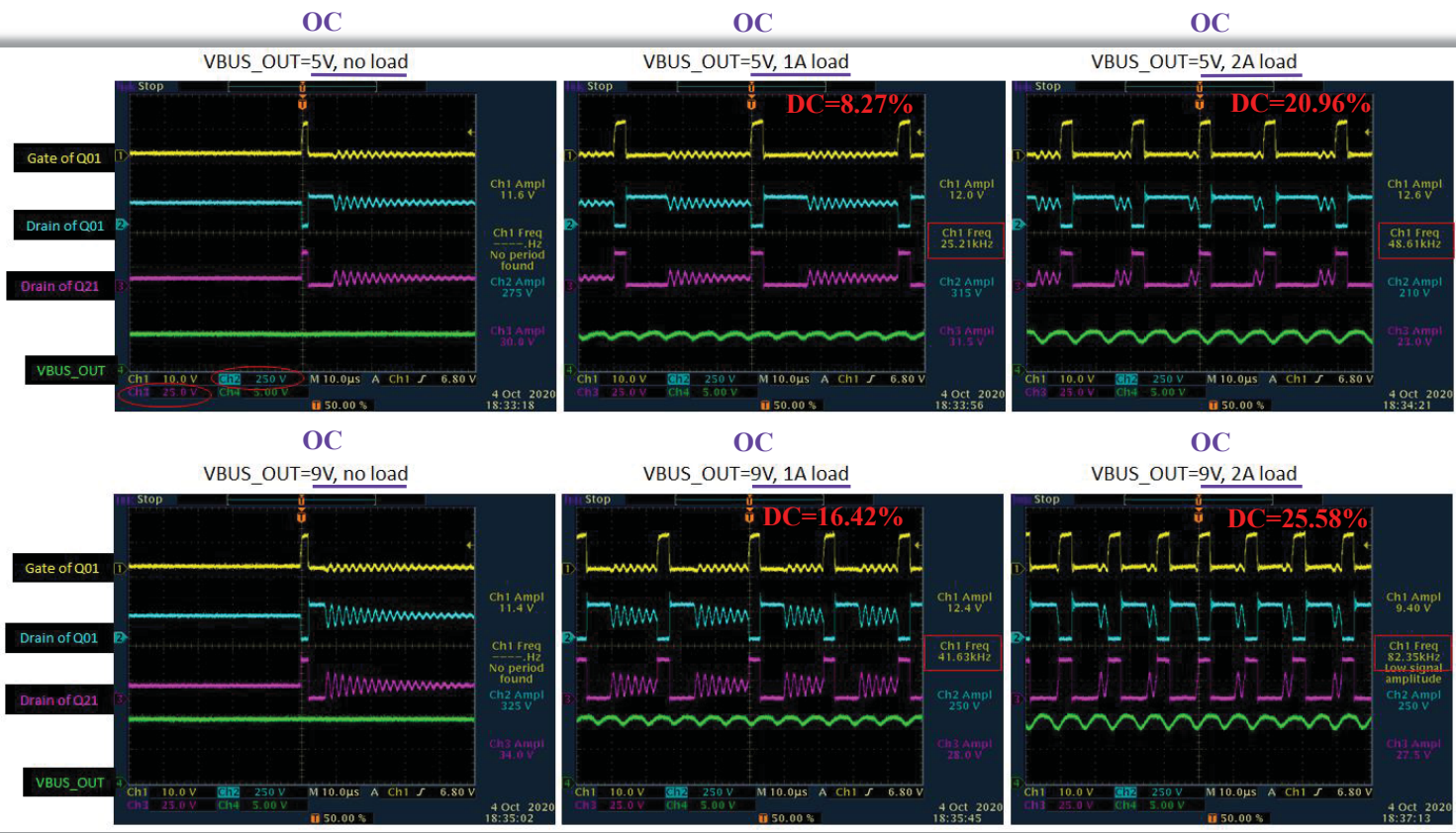| Pin Number	Pin Name	Type	Pin Description
1	GND	Ground	Ground.
2	DLNK	Analog Input	Digital communication link signal. Used for secondary-side to primary-side communication for all rapid change information, which includes output voltage requests, output current limits, output voltage undershoot, and over-voltage protection.
3	V$_{SENSE}$	Analog Input	Auxiliary voltage sense. Used for primary-side regulation and secondary-to-primary communication through main transformer.
4	CFG	Analog Input	Used for CDC configuration and auxiliary winding open protection.
5	I$_{SENSE}$	Analog Input	Primary-side current sense. Used for cycle-by-cycle peak-current control and limit in primary-side CV/CC regulation.
6	SOURCE	Power Input	Connect to the source of external power MOSFET. Inside the IC, it is connected to internal MOSFET and startup V$_{CC}$ charge circuit.
7	GATE	Output	Gate drive for external MOSFET switch.
8	V$_{CC}$	Power Input	IC power supply.

Source: Dialog Semiconductor iW1791 AC/DC Primary Side Rapid Charge PWM Controller with High Resolution Voltage/Current Control, Product Summary Rev. 1.51 05-OCT-2018, Note: The citation pertains to only the document excerpt not the schematics or other data.

| Claim 6	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800**

said controller further configured to provide a signal to control said **(DC) duty cycle** of said power switch as a function of said **(OC) output characteristic** and in accordance with said command,

OC
VBUS_OUT=5V, no load

OC
VBUS_OUT=5V, 1A load
DC=8.27%

OC
VBUS_OUT=5V, 2A load
DC=20.96%

OC
VBUS_OUT=9V, no load

OC
VBUS_OUT=9V, 1A load
DC=16.42%

OC
VBUS_OUT=9V, 2A load
DC=25.58%

| Claim 6 | **Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800** |

to provide a signal to control said **(DC) duty cycle** of said power switch as a function of said **(OC) output characteristic** and in accordance with command,
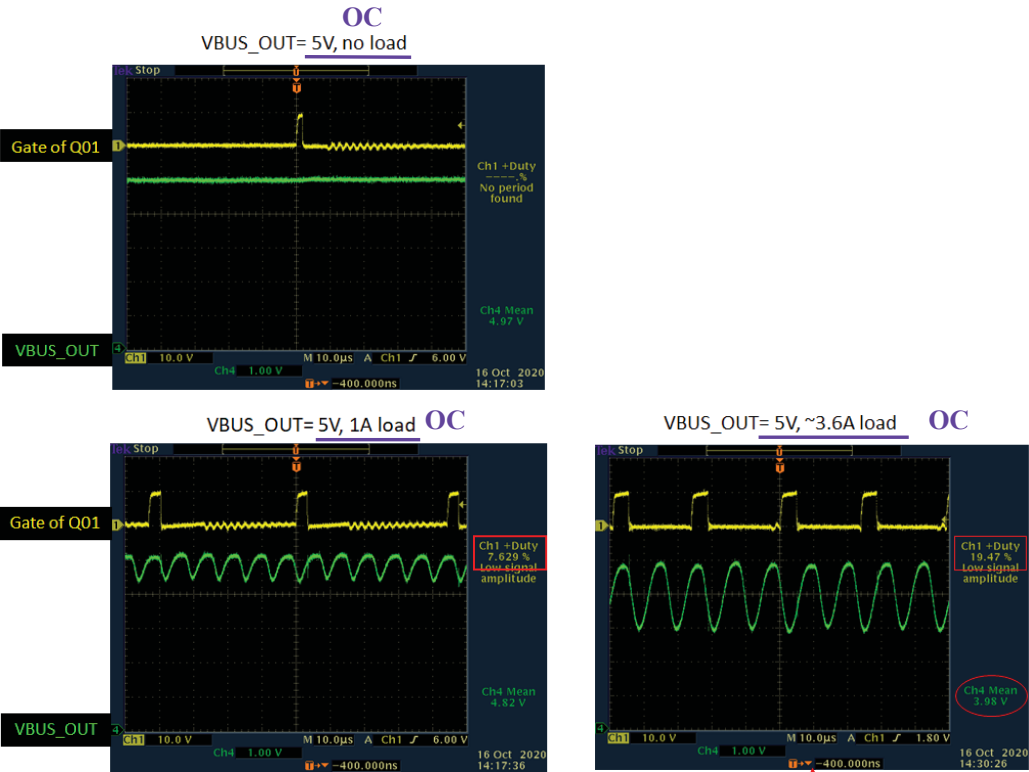
Note: The charger will hold up the VBUS_OUT voltage at ~4.5V under a 3.5A load but the charger shuts down when the load is increased beyond that. This O-scope capture was taken as the charger was going into one of those over-current protection shutdowns when the load was increased to ~3.6A. Immediately after this capture, the VBUS_OUT voltage drops to 0V.

Claim 6	Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800

thereby regulating an **(IOC) internal operating characteristic** of said **(CON) power converter** improve an operating efficiency thereof as a function of said **(OP) system operational state**.

CON

iW1791

AC/DC Primary-Side Rapid Charge™ PWM Controller
with High Resolution Voltage/Current Control

OP

Dialog's innovative proprietary technology ensures that power supplies designed with the iW1791 and Dialog's secondary-side controllers can provide output voltage configurations of 3V to 20V for USB PD, 5V/9V/12V for QC2.0 and 3.6V to 12V in 200mV increments for QC3.0 and other proprietary protocols.

IOC

- Proprietary optimized load adaptive maximum constant frequency PWM switching with quasi-resonant operation achieves best size, efficiency, and common mode noise

Source: Dialog Semiconductor iW1791 AC/DC Primary Side Rapid Charge PWM Controller with High Resolution Voltage/Current Control, Product Summary Rev. 1.51 05-OCT-2018, Note: The citation pertains to only the document excerpt not the schematics or other data.

Claim 6	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA800**

thereby regulating an internal operating characteristic of said power converter to **(EFF) improve an operating efficiency** thereof as a function of said **(OP) system operational state**.

<div align="center">

OP   **EFF**

</div>

			EP-TA800 (5V testing)				
vin	**I_in (A)**	**meas_W_in**	**V_out**	**I_out (A)**	**calc_W_out**	**meas_W_out**	**Efficiency**
	0.008	0.000	5.120	0.000	0.000	0.000	
	0.011	0.412	5.110	0.020	0.102	0.148	0.359
	0.021	0.800	5.100	0.100	0.510	0.522	0.653
	0.062	2.990	5.080	0.500	2.540	2.595	0.868
	0.101	5.550	5.070	1.000	5.070	5.109	0.921
	0.148	8.635	5.020	1.500	7.530	7.542	0.873
	0.185	11.240	5.000	2.000	10.000	9.983	0.888
	0.222	14.130	4.980	2.500	12.450	12.560	0.889
			EP-TA800 (9V testing)				
vin	**I_in (A)**	**meas_W_in**	**V_out**	**I_out (A)**	**calc_W_out**	**meas_W_out**	**Efficiency**
	0.015	0.554	9.140	0.000	0.000	0.000	
	0.022	0.858	9.130	0.020	0.183	0.266	0.310
	0.035	1.521	9.130	0.100	0.913	0.933	0.613
	0.099	5.399	9.100	0.500	4.550	4.650	0.861
	0.171	10.210	9.090	1.000	9.090	9.152	0.896
	0.241	15.230	9.080	1.500	13.620	13.640	0.896
	0.305	19.670	9.000	2.000	18.000	18.060	0.918
	0.375	24.830	8.990	2.500	22.475	22.680	0.913
	0.437	30.450	8.970	3.000	26.910	27.035	0.888

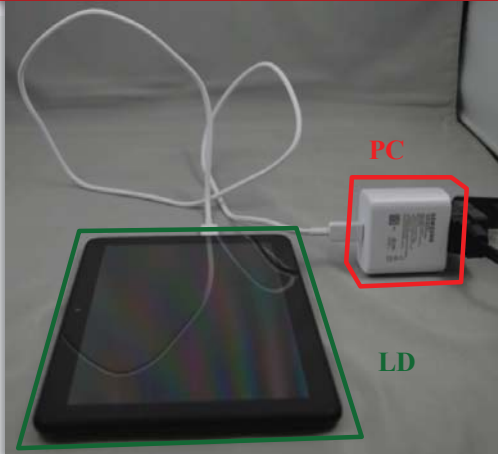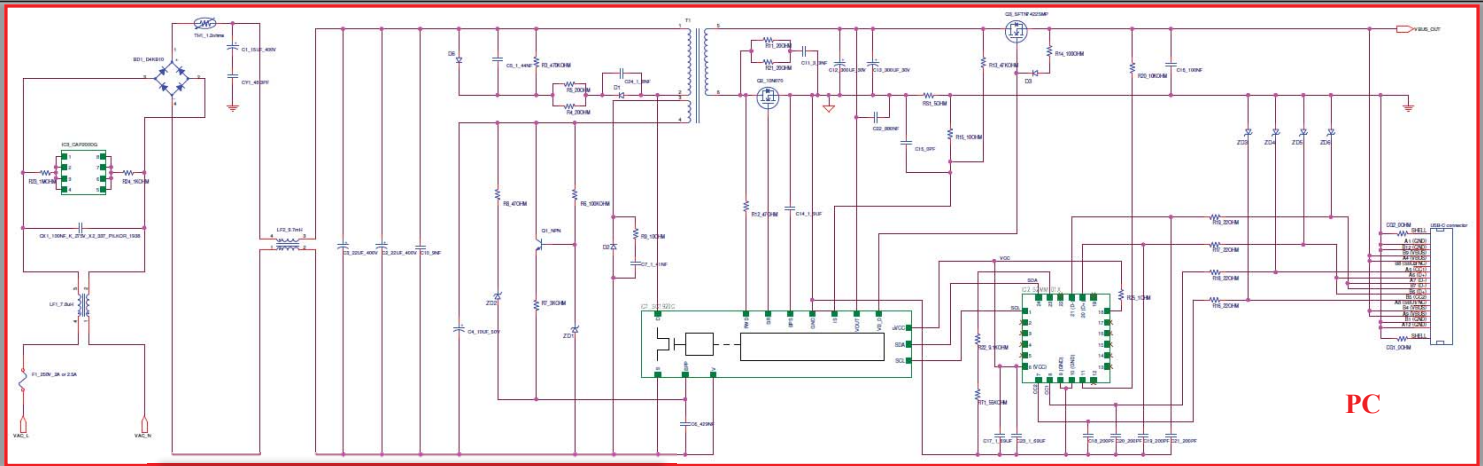**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845**

Claim 1

A **(PC) power converter** coupled to a **(PCC) power system controller configured to receive** a **(S) signal** indicating a **(OP) system operational state** of a **(LD) load** coupled thereto, comprising:

a **(PS) power switch configured to conduct for** a **(DC) duty cycle** to provide a **(OC) regulated output characteristic** at an **(OUT) output** thereof; and

a **(CON) controller configured to receive** a **(COM) command** from said **(PCC) power system controller** to enter a **(PCOP) power converter operational state**

as a function of said **(S) signal** indicating said **(OP) system operational state**,

said **(CON) controller further configured to provide** a **(OS) signal to control** said **(DC) duty cycle** of said **(PS) power switch** as a function of said **(OC) output characteristic** and in accordance with said **(COM) command**, thereby regulating an **(IOC) internal operating characteristic** of said **(PC) power converter** to improve an operating efficiency thereof as a function of said **(OP) system operational state**.

Claim 1	Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845

A **(PC) power converter** coupled to a power system controller configured to receive a signal indicating a system operational state of a **(LD) load** coupled thereto, comprising:
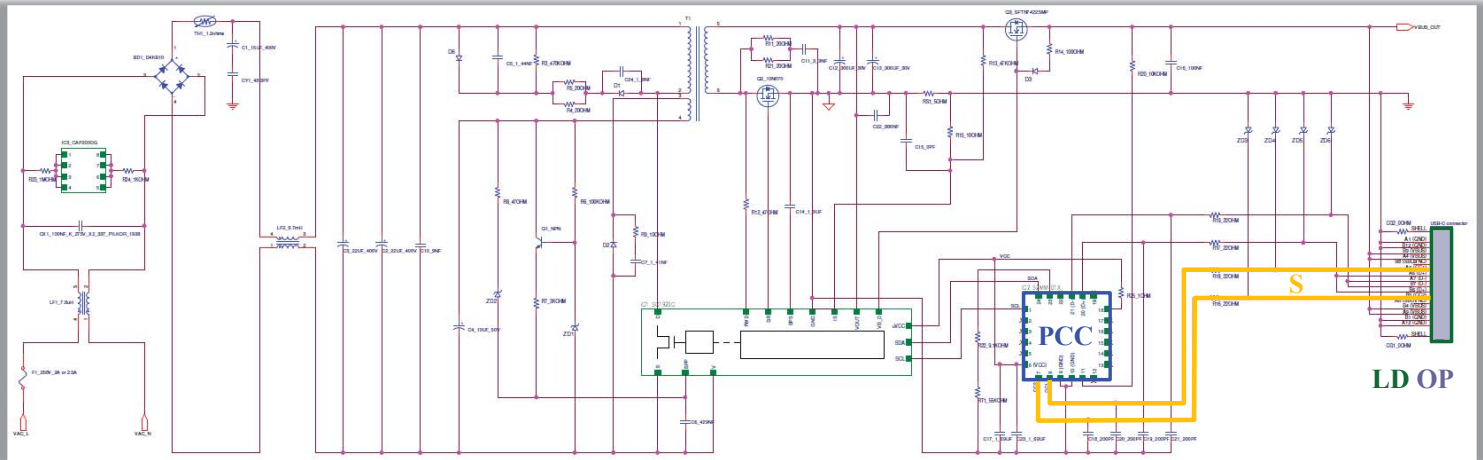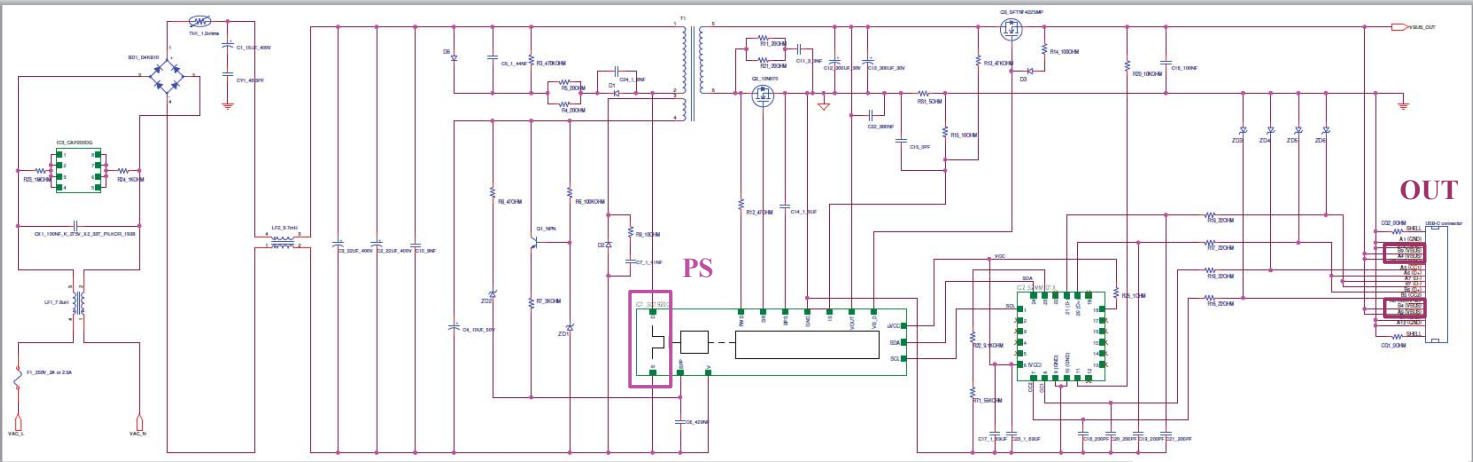
| Claim 1 | **Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845** |

A power converter coupled to a **(PCC) power system controller configured to receive** a **(S) signal** indicating a **(OP) system operational state** of a **(LD) load** coupled thereto, comprising:

| Claim 1 | **Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845** |

A power converter coupled to a power system controller configured to receive a **(S) signal** indicating a **(OP) system operational state** of a load coupled thereto, comprising:

OP

VBUS_OUT= 5V (no load), then transitions to 9V (no load)

Pin 24 (Drain) of IC1

S

CC1

This burst of data was fed to CC1 by the external PD3.0 emulator, immediately after pressing its trigger button that sends the charger a request for 9V output at VBUS_OUT.

CC2

9V

5V

VBUS_OUT

Shown at 20ms/div scale in order to capture the entire transition from 5V to 9V at VBUS_OUT.

Claim 1	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845**

a **(PS) power switch configured to conduct for** a duty cycle to provide a **(OC) regulated output characteristic** at an **(OUT) output** thereof; and

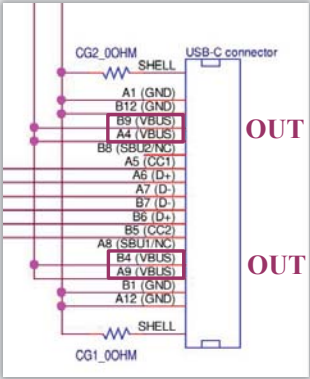
PS

OUT

4.5   Configuration Channel (CC)

4.5.1   Architectural Overview

For the USB Type-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the Source-to-Sink connection. When the device is connected through a hub, the connection between a Sink (UFP) on the hub and the Source (host port) and the connection between the Sink (device port) and a Source (DFP on the hub), are treated as separate connections. Functionally, the configuration channel is used to serve the following purposes.

- Detect attach of USB ports, e.g. a Source to a Sink
- Resolve cable orientation and twist connections to establish USB data bus routing
- Establish data roles between two attached ports   **OC**
- Discover and configure VBUS: USB Type-C Current modes or *USB Power Delivery*
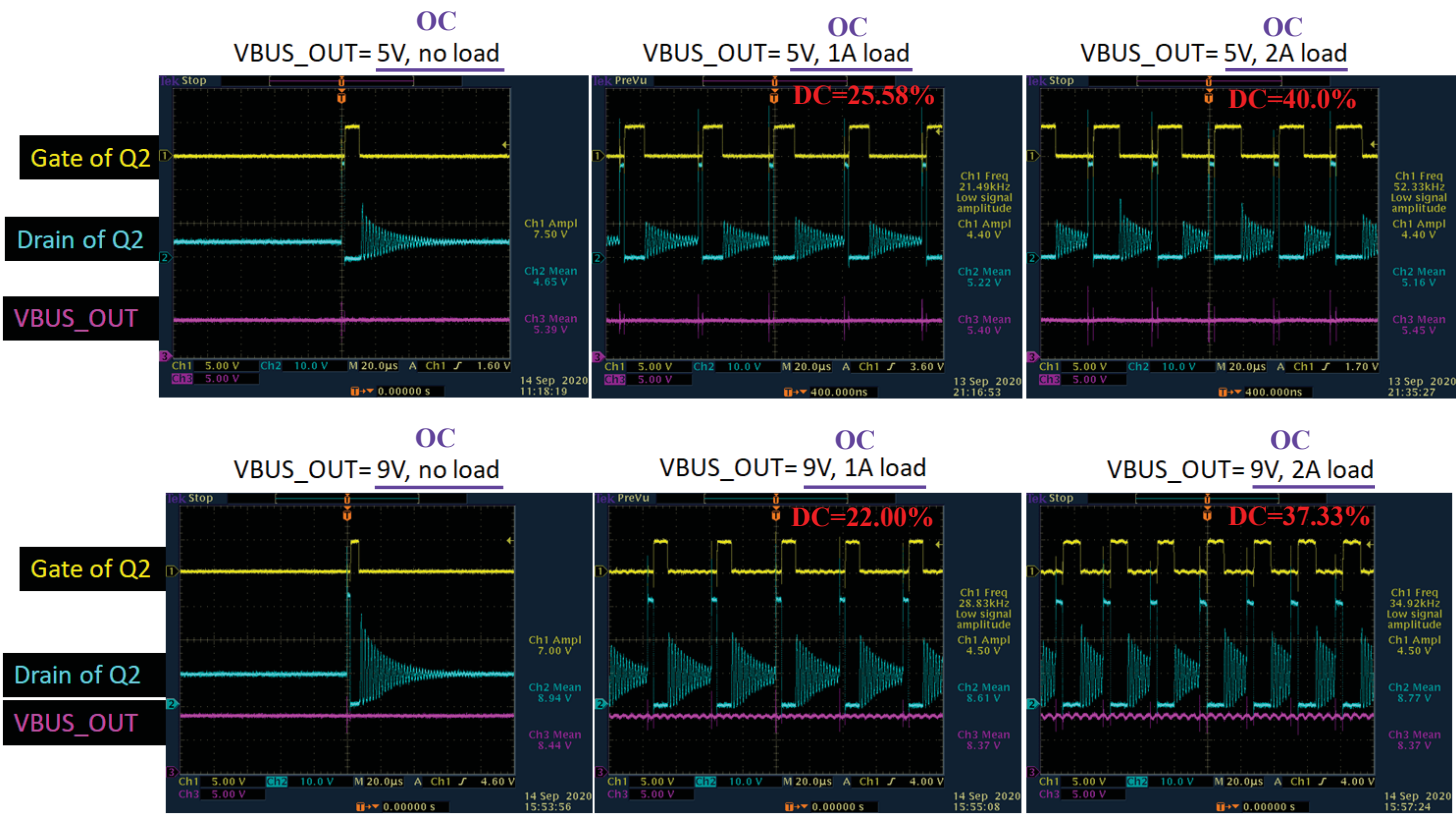

OUT

OUT

Source: https://usb.org/sites/default/files/USB%20Type-C%20Spec%20R2.0%20-%20August%202019.pdf, Note: The citation pertains to only the document excerpt not the schematics or other data.

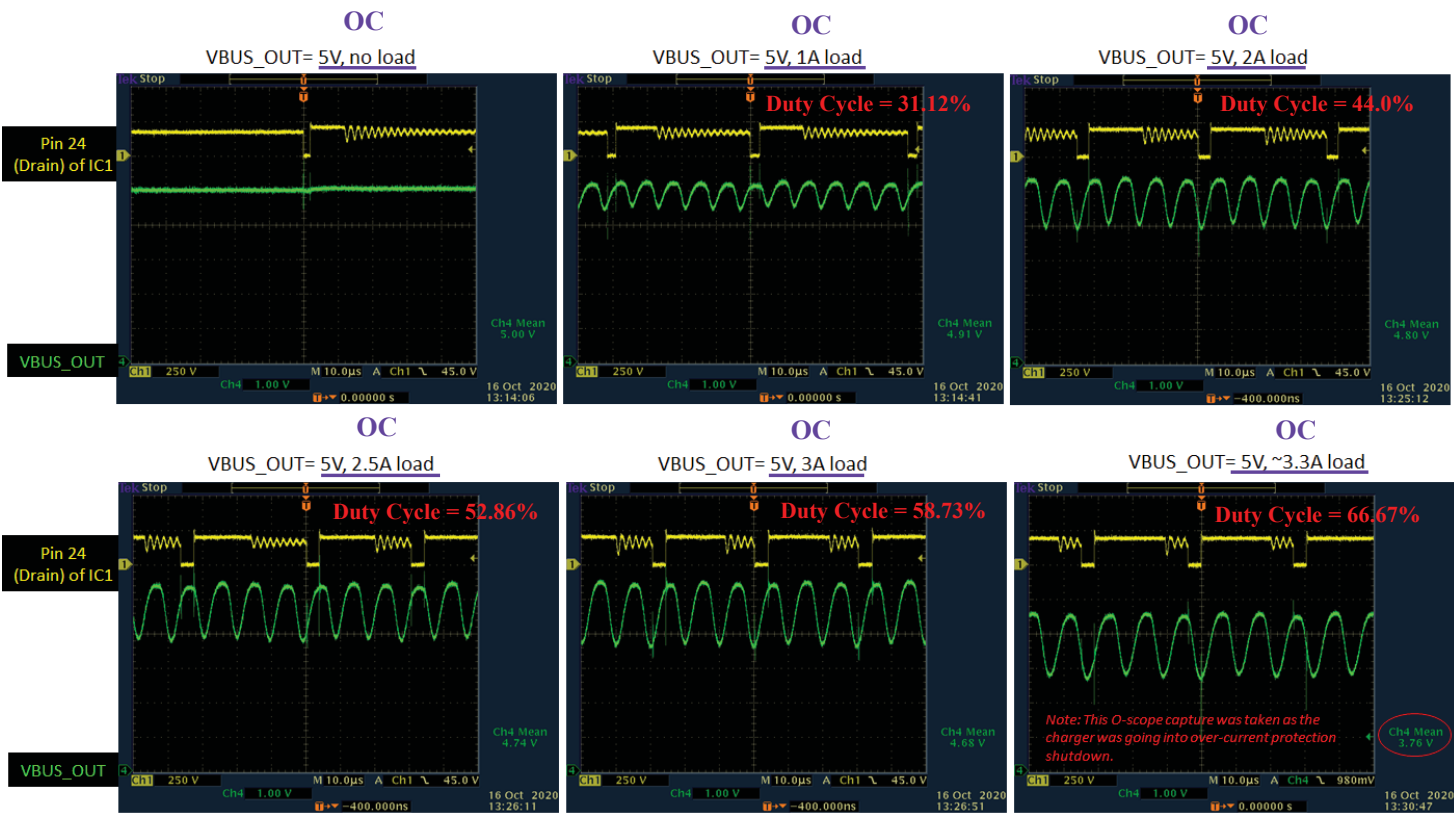| Claim 1	Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845

a power switch configured to conduct for a **(DC) duty cycle** to provide an **(OC) output characteristic** at an output thereof; and

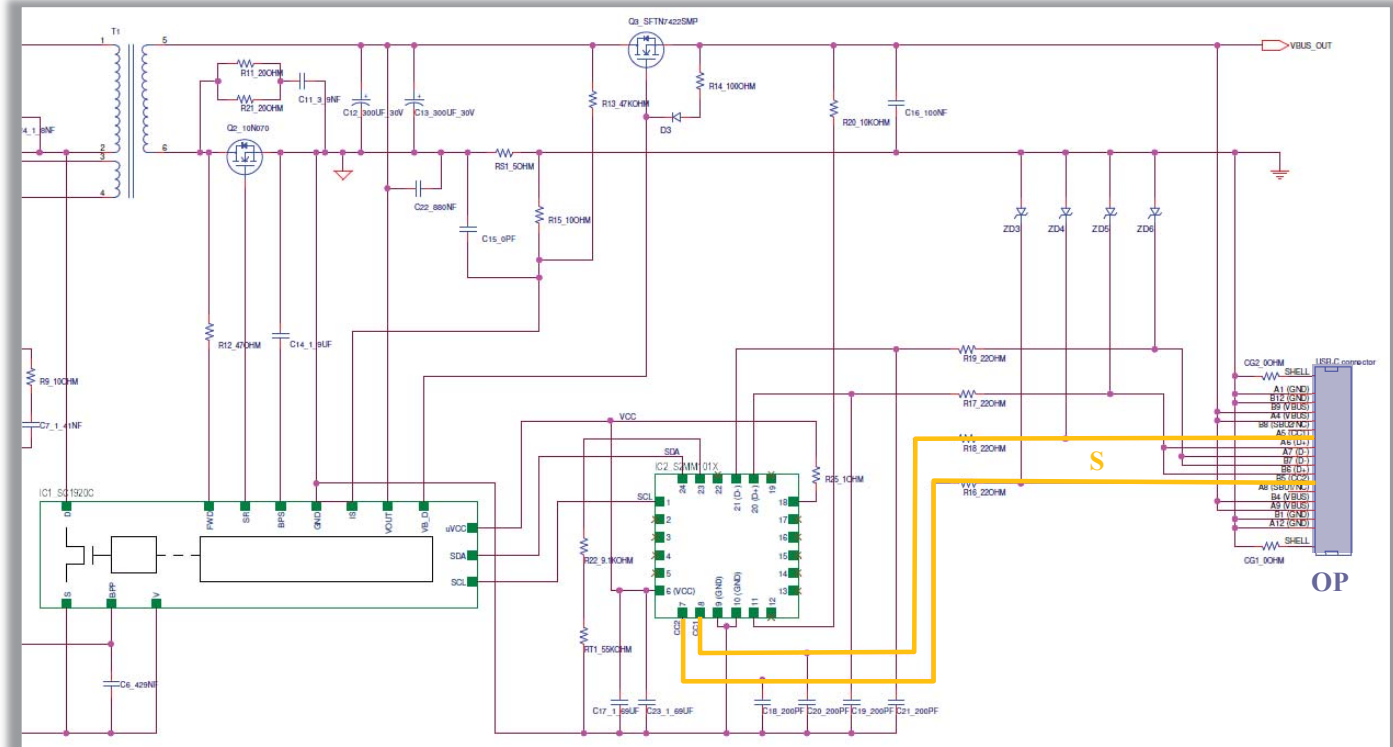| Claim 1	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845**

a power switch configured to conduct for a **(DC) duty cycle** to provide an **(OC) output characteristic** at an output thereof; and

Claim 1	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845**

a **(CON) controller configured to receive** a **(COM) command** from said **(PCC) power system controller** to enter a **(PCOP) power converter operational state**

Claim 1	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845**

as a function of said **(S) signal** indicating said **(OP) system operational state**,

Source: InnoSwitch3-Pro Family, Rev. M 8/20,
Note: The citation pertains to only the document
excerpt not the schematics or other data.

OP

Highly Integrated, Compact Footprint
- Multi-mode Quasi-Resonant (QR) / DCM / CCM flyback controller, high-voltage switch, secondary-side sensing and synchronous rectifier driver
- Optimized efficiency across line and load range

Claim 1	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845**

as a function of said **(S) signal** indicating said **(OP) system operational state**,
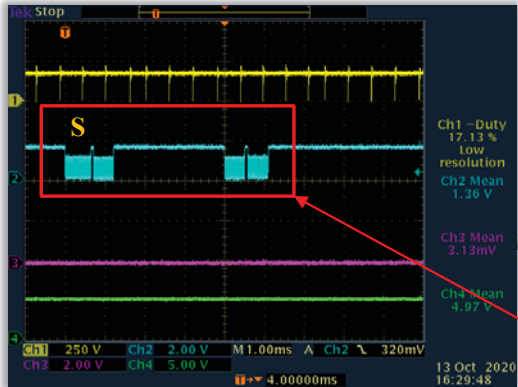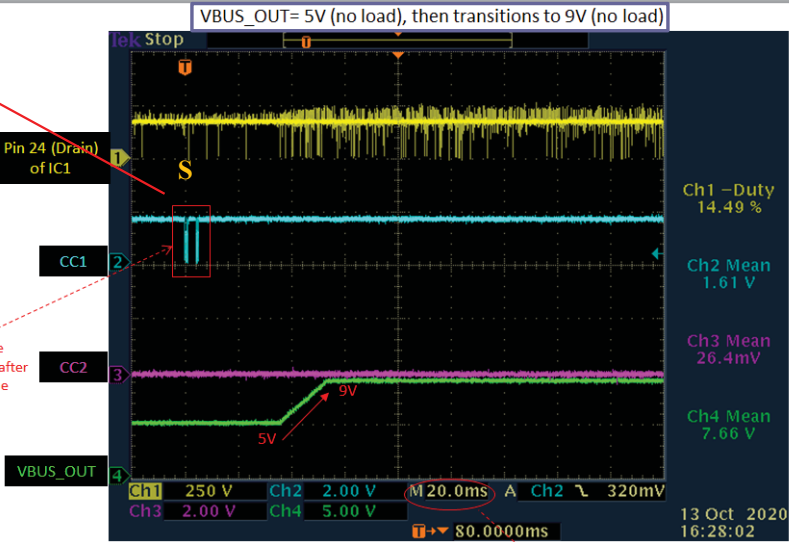
| Claim 1 | Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845 |

said **(CON) controller further configured to provide** a **(OS) signal to control** said duty cycle of said **(PS) power switch** as a function of said output characteristic and in accordance with said **(COM) command**,
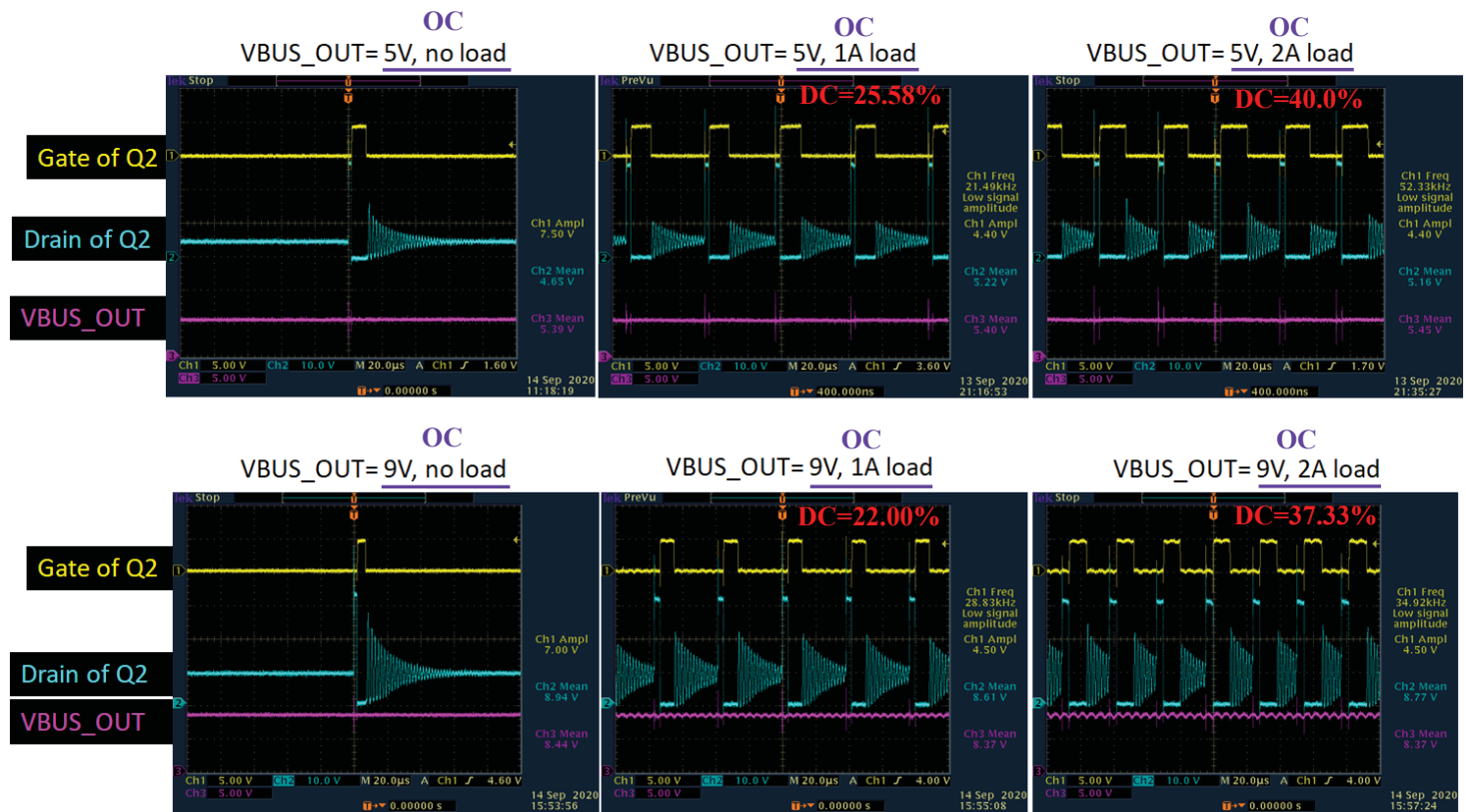
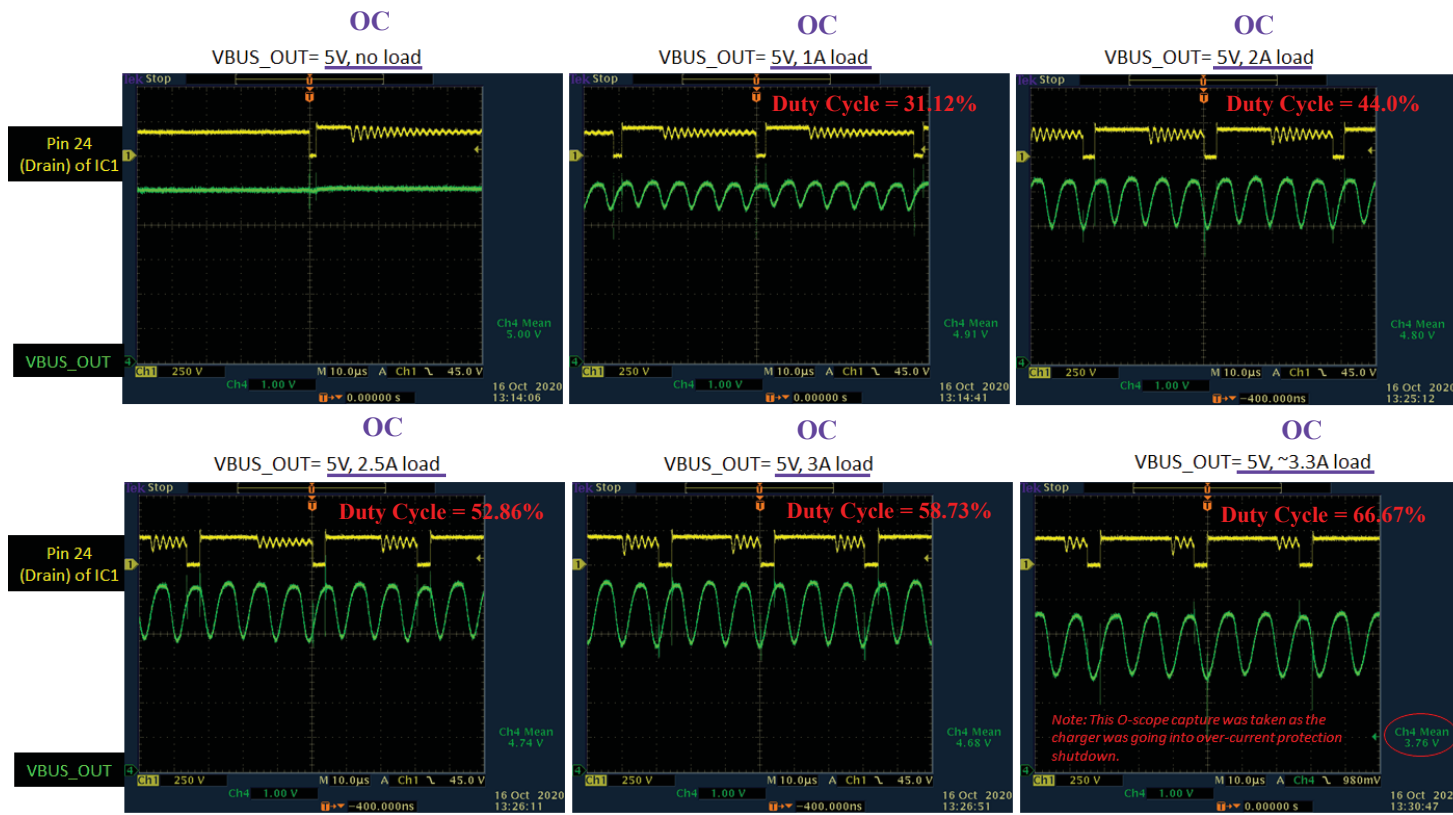| Claim 1 | **Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845** |

said controller further configured to provide a signal to control said **(DC) duty cycle** of said power switch as a function of said **(OC) output characteristic** and in accordance with said command,

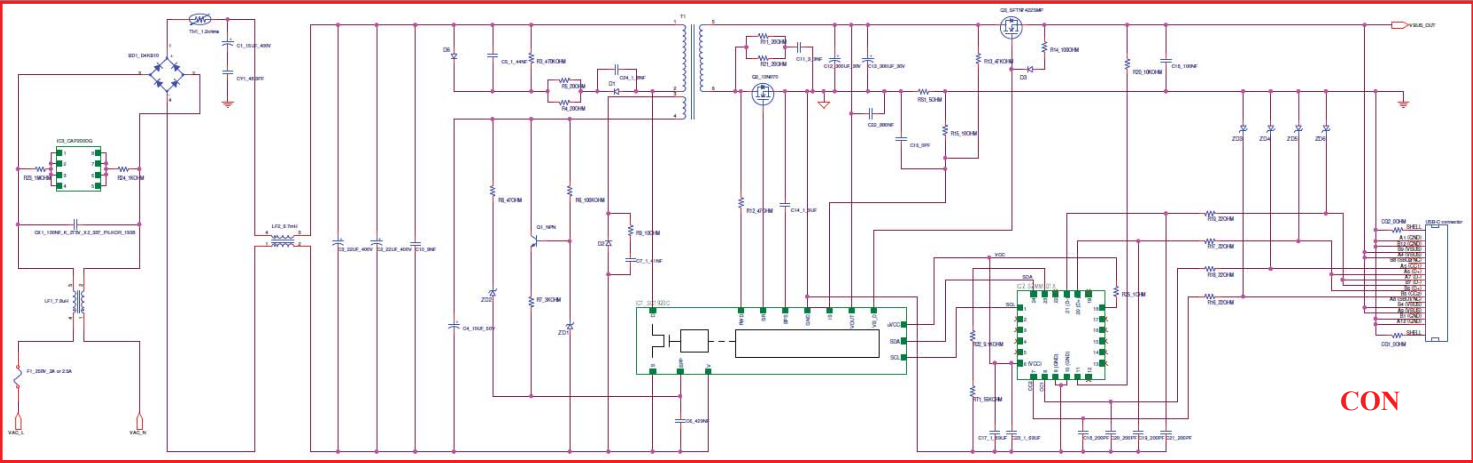| Claim 1	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845**

said controller further configured to provide a signal to control said **(DC) duty cycle** of said power switch as a function of said **(OC) output characteristic** and in accordance with said command,

Claim 1	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845**

thereby regulating an **(IOC) internal operating characteristic** of said **(PC) power converter** to improve an operating efficiency thereof as a function of said **(OP) system operational state**.

CON

OP

IOC

Highly Integrated, Compact Footprint
- Multi-mode Quasi-Resonant (QR) / DCM / CCM flyback controller, high-voltage switch, secondary-side sensing and synchronous rectifier driver
- Optimized efficiency across line and load range
- Integrated FluxLink™, HIPOT-isolated, feedback link
- Instantaneous transient response
- Drives low-cost N-channel FET series load switch
- Integrated 3.6 V supply for external MCU

Source: InnoSwitch3-Pro Family, Rev. M 8/20, Note: The citation pertains to only the document excerpt not the schematics or other data.

Claim 1	Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845

thereby regulating an internal operating characteristic of said power converter to **(EFF) improve an operating efficiency** thereof as a function of said **(OP) system operational state**.

OP   **EFF**

			EP-TA845 (5v testing)			
vin	I_in (A)	meas_W_in	V_out	I_out (A)	calc_W_out	meas_W_out	Efficiency
	0.008	0.000	5.040	0.000	0.000	0.000	
	0.011	0.346	5.040	0.020	0.101	0.146	0.422
	0.021	0.745	5.040	0.100	0.504	0.513	0.689
	0.063	2.886	5.010	0.500	2.505	2.554	0.885
	0.106	5.472	4.970	1.000	4.970	4.995	0.913
	0.165	8.330	4.920	1.500	7.380	7.432	0.892
	0.194	11.040	4.920	2.000	9.840	9.860	0.893
	0.233	13.760	4.850	2.500	12.125	12.290	0.893
			EP-TA845 (9V testing)			
vin	I_in (A)	meas_W_in	V_out	I_out (A)	calc_W_out	meas_W_out	Efficiency
	0.015	0.508	8.990	0.000	0.000	0.000	
	0.021	0.732	8.990	0.020	0.180	0.261	0.357
	0.036	1.415	8.970	0.100	0.897	0.916	0.647
	0.108	5.206	8.940	0.500	4.470	4.570	0.878
	0.193	9.804	8.910	1.000	8.910	9.030	0.921
	0.247	14.570	8.840	1.500	13.260	13.270	0.911
	0.314	19.410	8.820	2.000	17.640	17.640	0.909
	0.381	24.100	8.740	2.500	21.850	21.860	0.907
	0.441	28.730	8.710	3.000	26.130	26.110	0.909

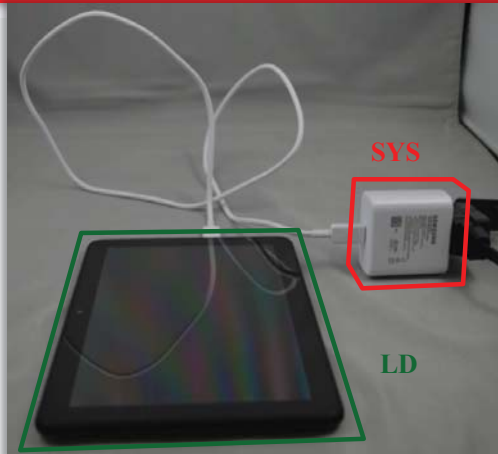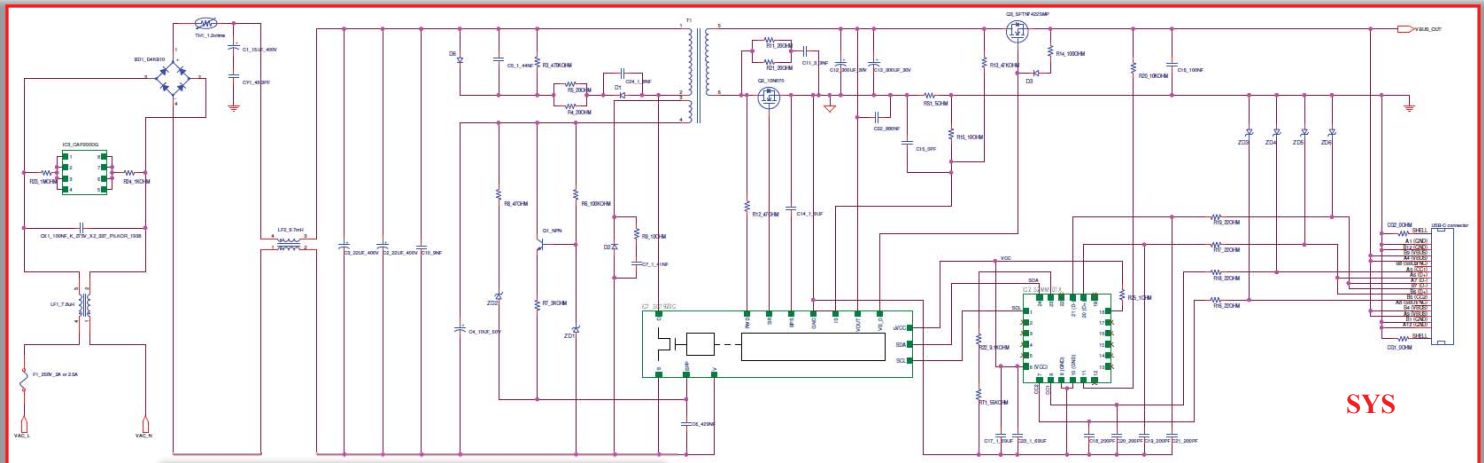**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845**

Claim 6

A **(SYS) power system** coupled to a **(LD) load**, comprising:

a **(PCC) power system controller configured to receive** a **(S) signal** indicating a **(OP) system operational state** of said **(LD) load** and

to select a **(PCOP) power converter operational state** as a function thereof; and

a **(CON) power converter**, including:

a **(PS) power switch configured to conduct for** a **(DC) duty cycle** to provide a **(OC) regulated output characteristic** at an **(OUT) output** thereof, and

a **(CON) controller configured to receive** a **(COM) command** from said **(PCC) power system controller** to enter said **(PCOP) power converter operational state** and

to provide a **(S) signal to control** said **(DC) duty cycle** of said **(PS) power switch** as a function of said **(OC) output characteristic** and in accordance with said **(COM) command,**

thereby regulating an **(IOC) internal operating characteristic** of said **(CON) power converter** to **(EFF) improve an operating efficiency thereof** as a function of said **(OP) system operational state**.

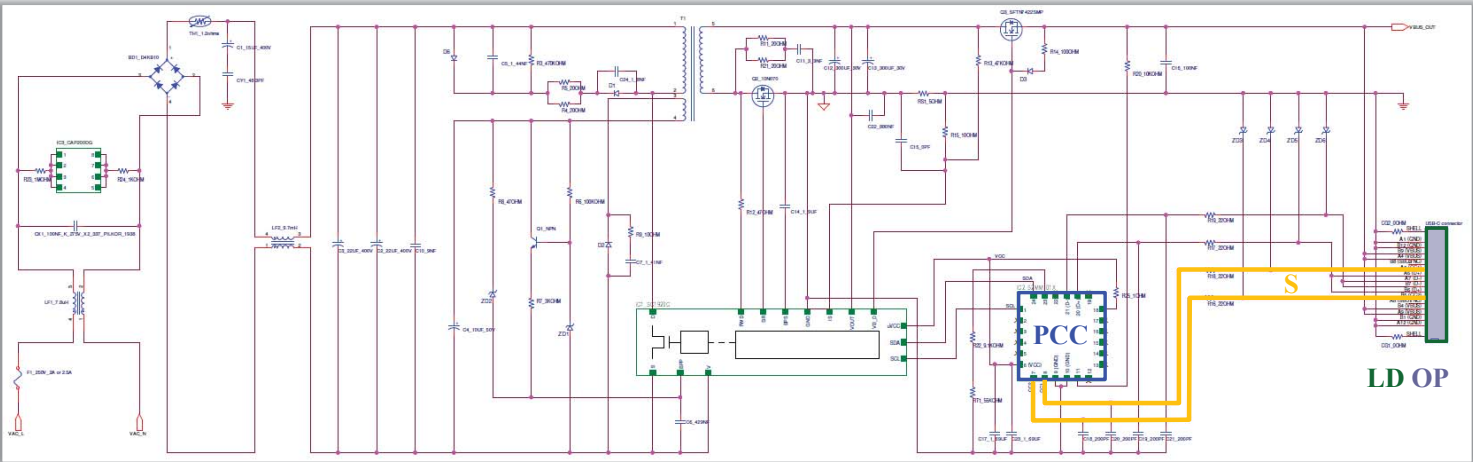| Claim 6	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845**

A **(SYS) power system** **coupled to** a **(LD) load**, comprising:

Claim 6	Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845

a **(PCC) power system controller configured to receive** a **(S) signal** indicating a **(OP) system operational state** of said **(LD) load** and

OP

Highly Integrated, Compact Footprint
- Multi-mode Quasi-Resonant (QR) / DCM / CCM flyback controller, high-voltage switch, secondary-side sensing and synchronous rectifier driver
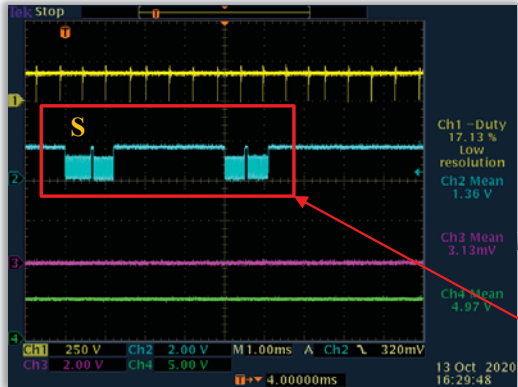- Optimized efficiency across line and load range

Source: InnoSwitch3-Pro Family, Rev. M 8/20, Note: The citation pertains to only the document excerpt not the schematics or other data.
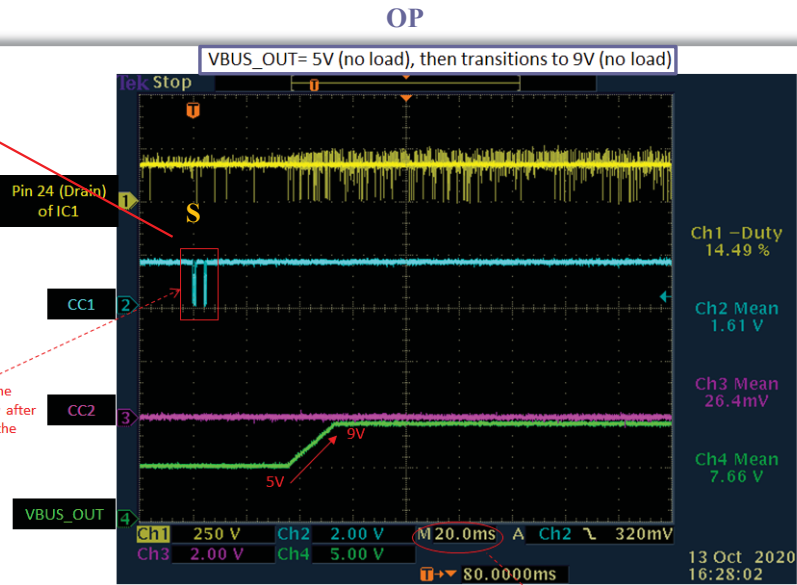
Claim 6	Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845

a power system controller configured to receive a **(S) signal** indicating a **(OP) system operational state** of said load and

OP

VBUS_OUT= 5V (no load), then transitions to 9V (no load)

Pin 24 (Drain) of IC1

S

CC1

This burst of data was fed to CC1 by the external PD3.0 emulator, immediately after pressing its trigger button that sends the charger a request for 9V output at VBUS_OUT.
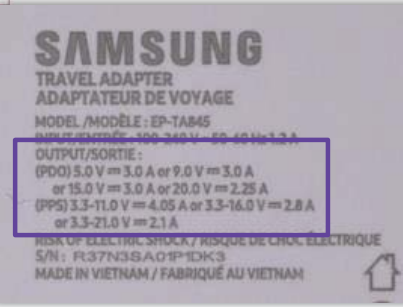
CC2

9V

5V

VBUS_OUT

Shown at 20ms/div scale in order to capture the entire transition from 5V to 9V at VBUS_OUT.

Claim 6	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845**

to select a **(PCOP) power converter operational state** as a function thereof; and
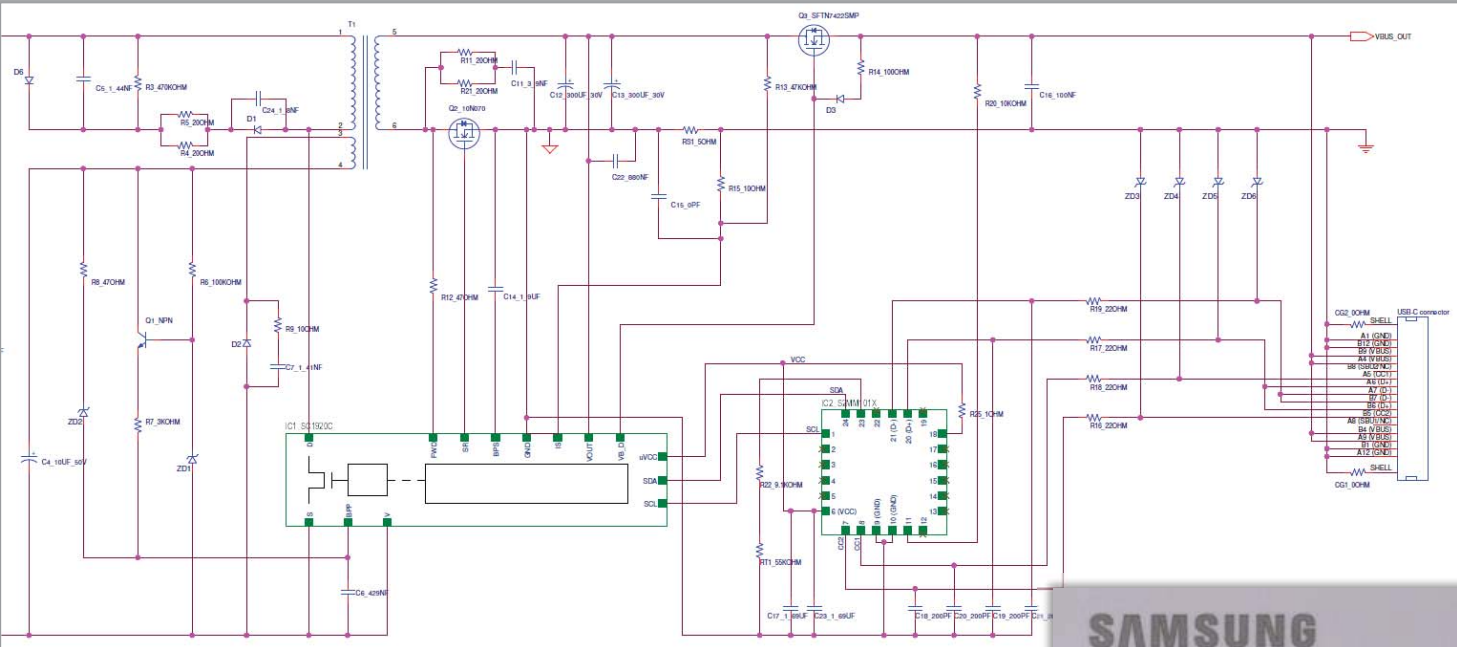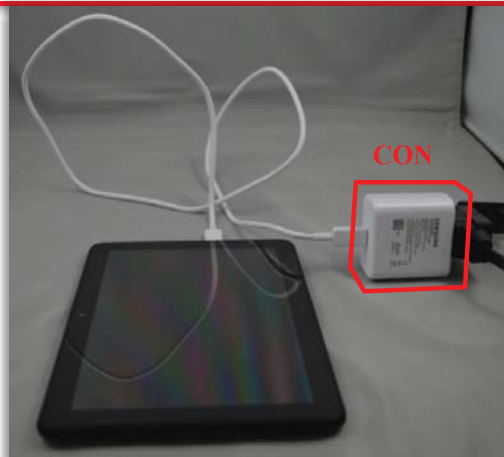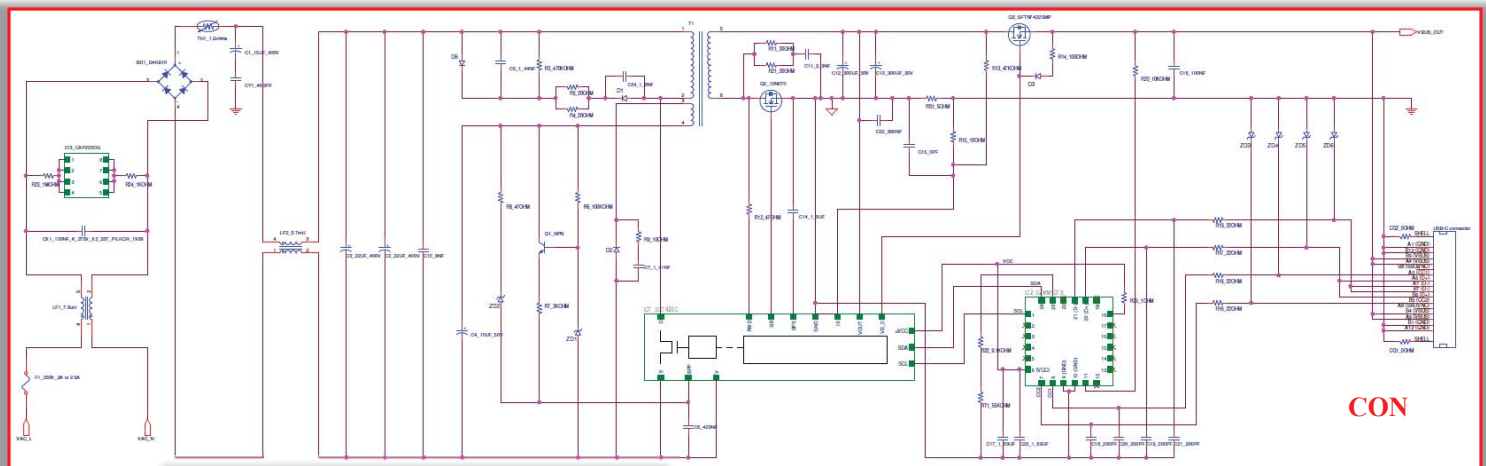

PCOP

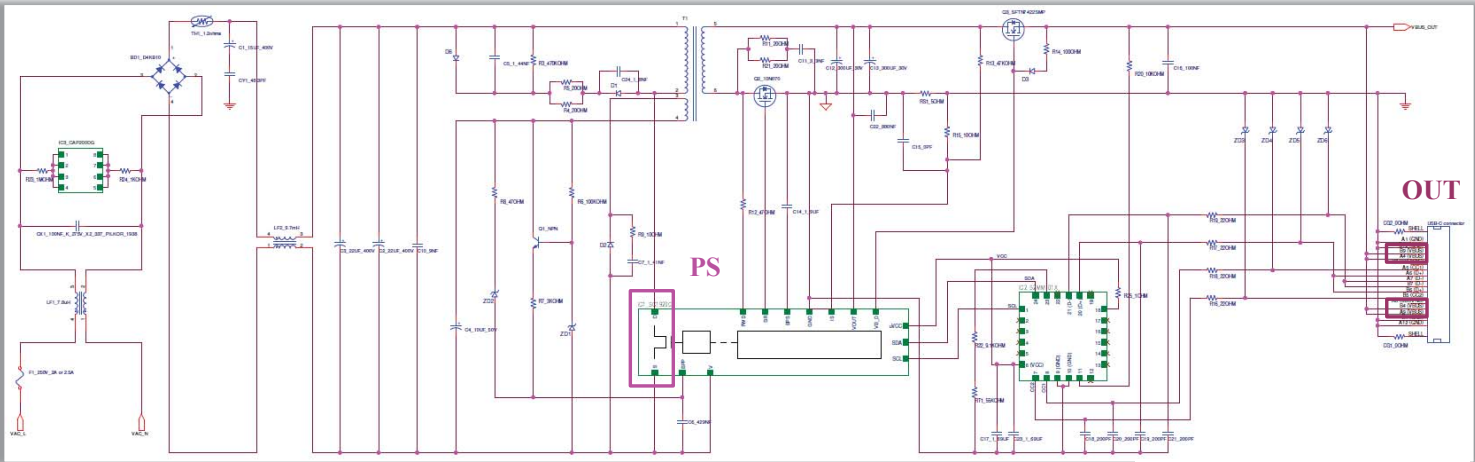| Claim 6	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845**

a **(CON) power converter**, including:

Claim 6	Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845

a **(PS) power switch configured to conduct for** a duty cycle to provide a **(OC) regulated output characteristic** at an **(OUT) output** thereof, and
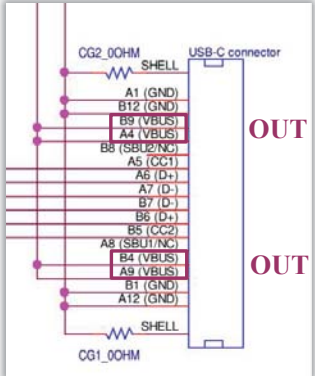

OUT

PS

4.5   Configuration Channel (CC)

4.5.1   Architectural Overview

For the USB Type-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the Source-to-Sink connection. When the device is connected through a hub, the connection between a Sink (UFP) on the hub and the Source (host port) and the connection between the Sink (device port) and a Source (DFP on the hub), are treated as separate connections. Functionally, the configuration channel is used to serve the following purposes.

- Detect attach of USB ports, e.g. a Source to a Sink
- Resolve cable orientation and twist connections to establish USB data bus routing
- Establish data roles between two attached ports   **OC**
- Discover and configure VBUS: USB Type-C Current modes or *USB Power Delivery*
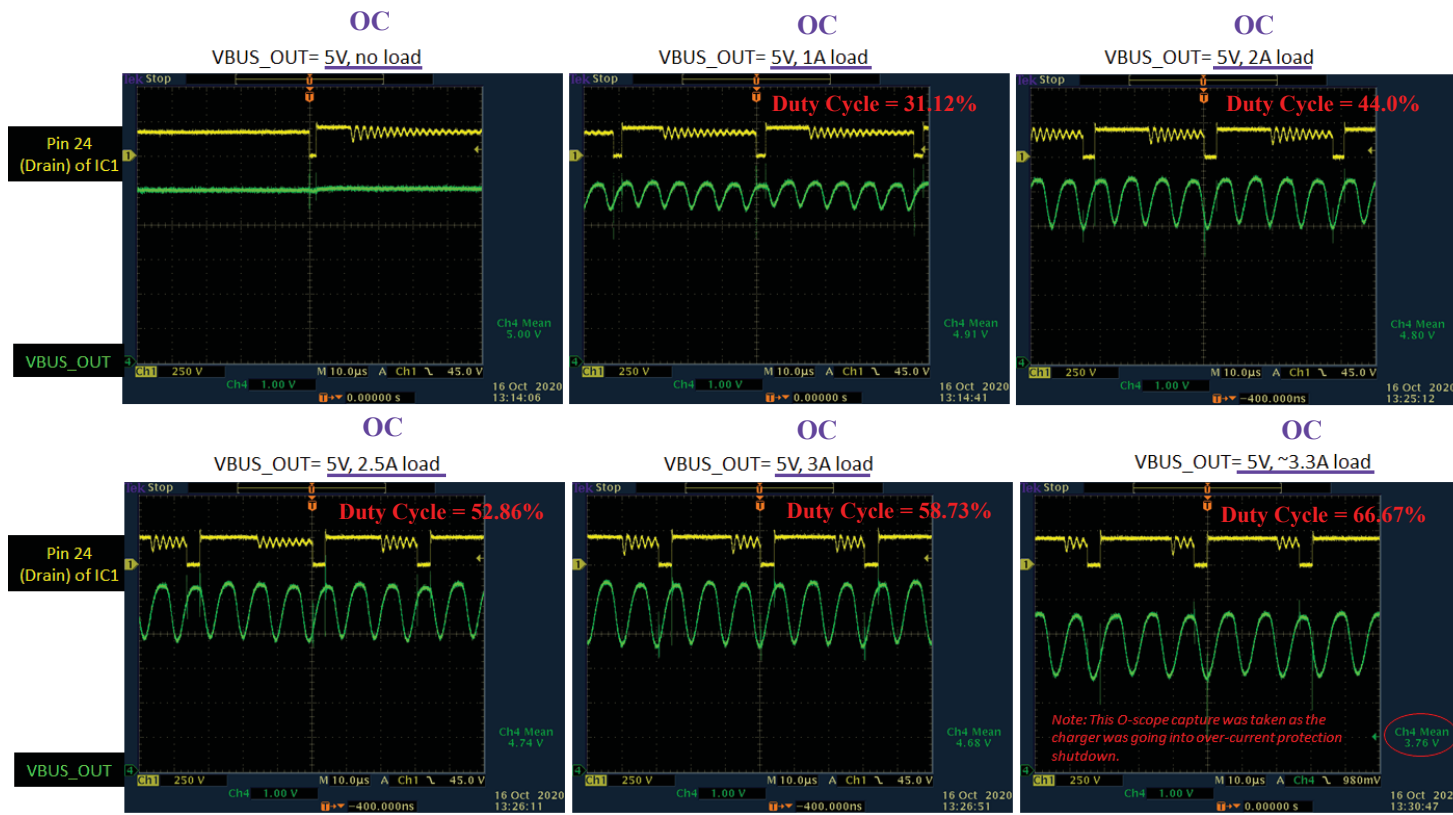

OUT

OUT

Source: https://usb.org/sites/default/files/USB%20Type-C%20Spec%20R2.0%20-%20August%202019.pdf, Note: The citation pertains to only the document excerpt not the schematics or other data.

Claim 6	Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845

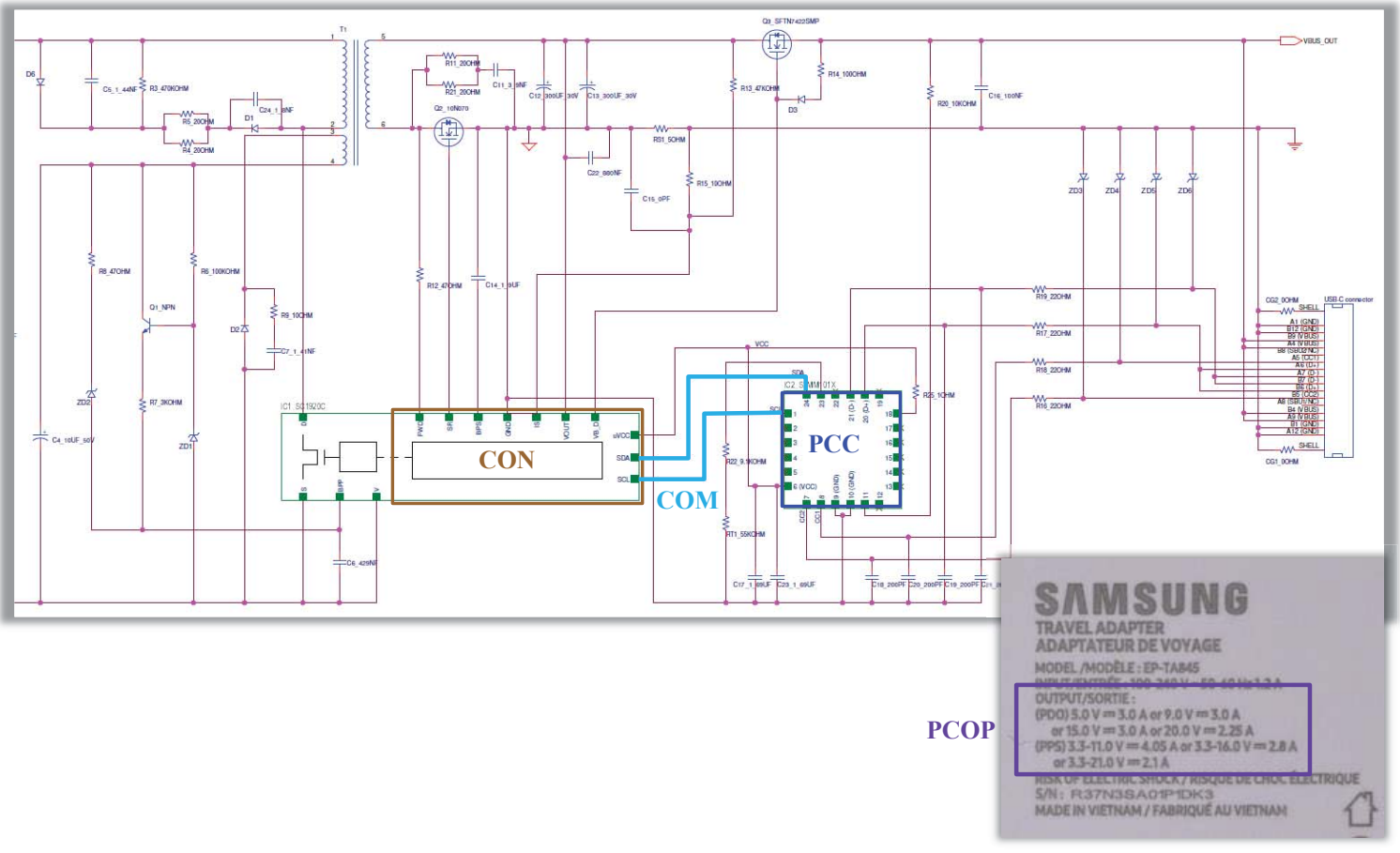a power switch configured to conduct for a **(DC) duty cycle** to provide a **(OC) regulated output characteristic** at an output thereof, and

Claim 6	Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845

a **(CON) controller configured to receive** a **(COM) command** from said **(PCC) power system controller** to enter said **(PCOP) power converter operational state** and

<table>
<tr><td>Claim 6</td><td style="text-align:center">Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845</td></tr>
</table>

to provide a **(OS) signal to control** said duty cycle of said **(PS) power switch** as a function of said output characteristic and in accordance with said **(COM) command**,
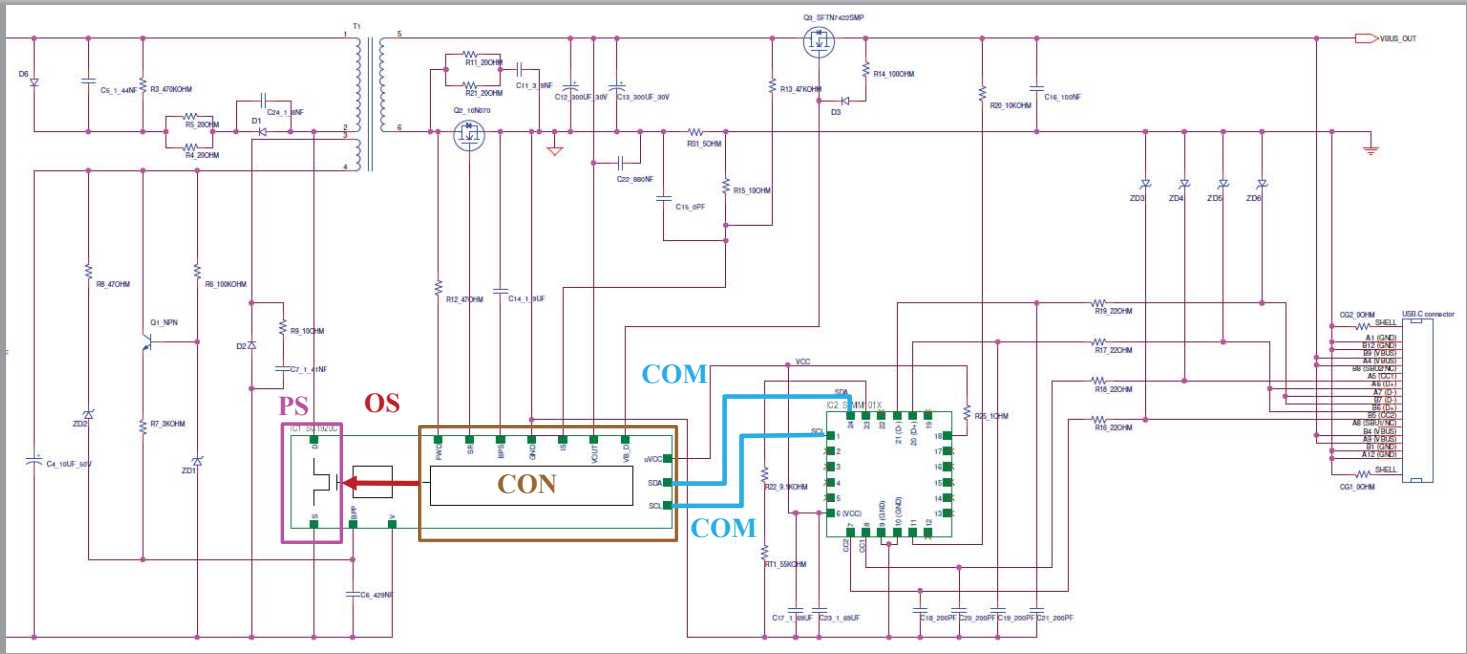
Claim 6	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845**

said controller further configured to provide a signal to control said **(DC) duty cycle** of said power switch as a function of said **(OC) output characteristic** and in accordance with said command,

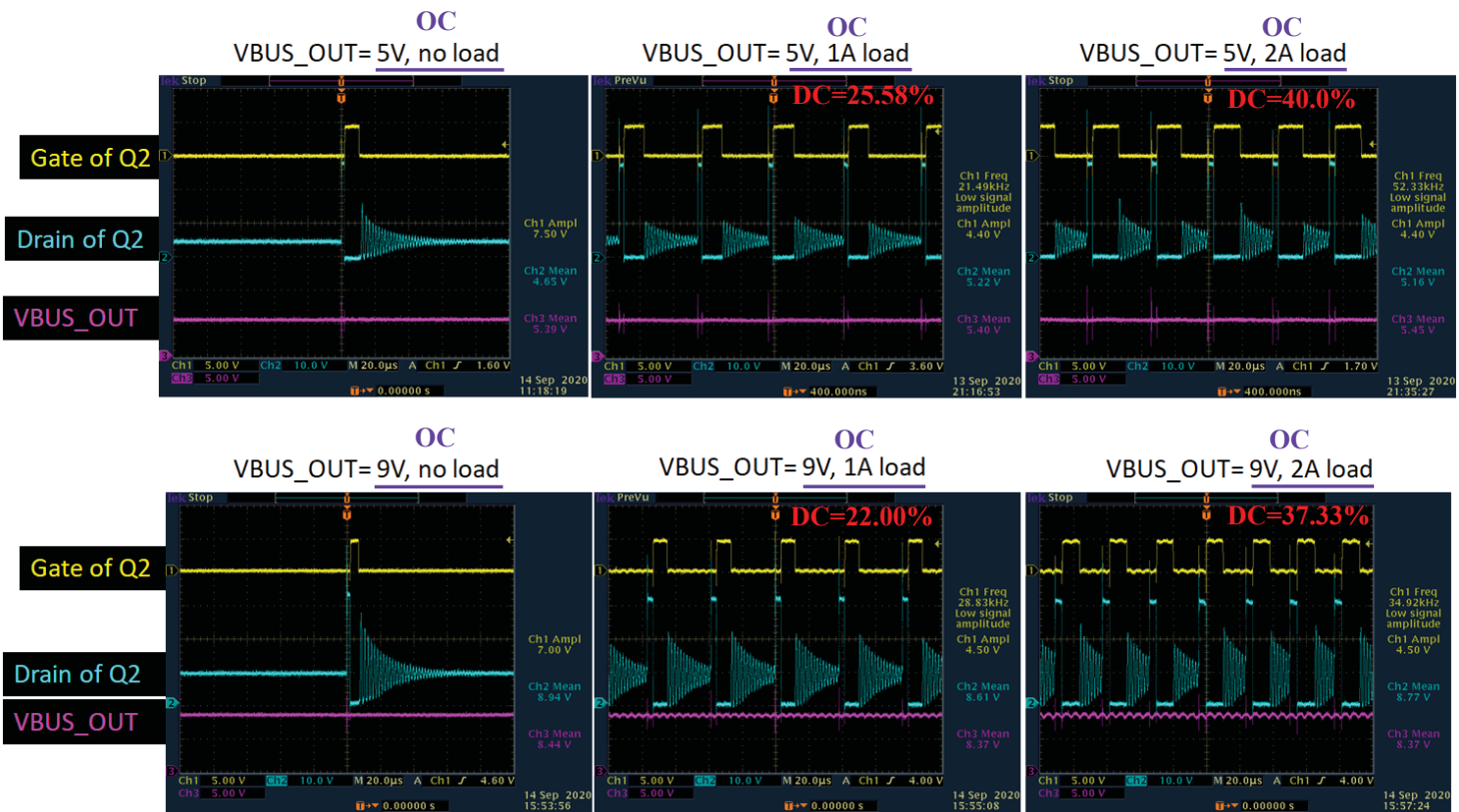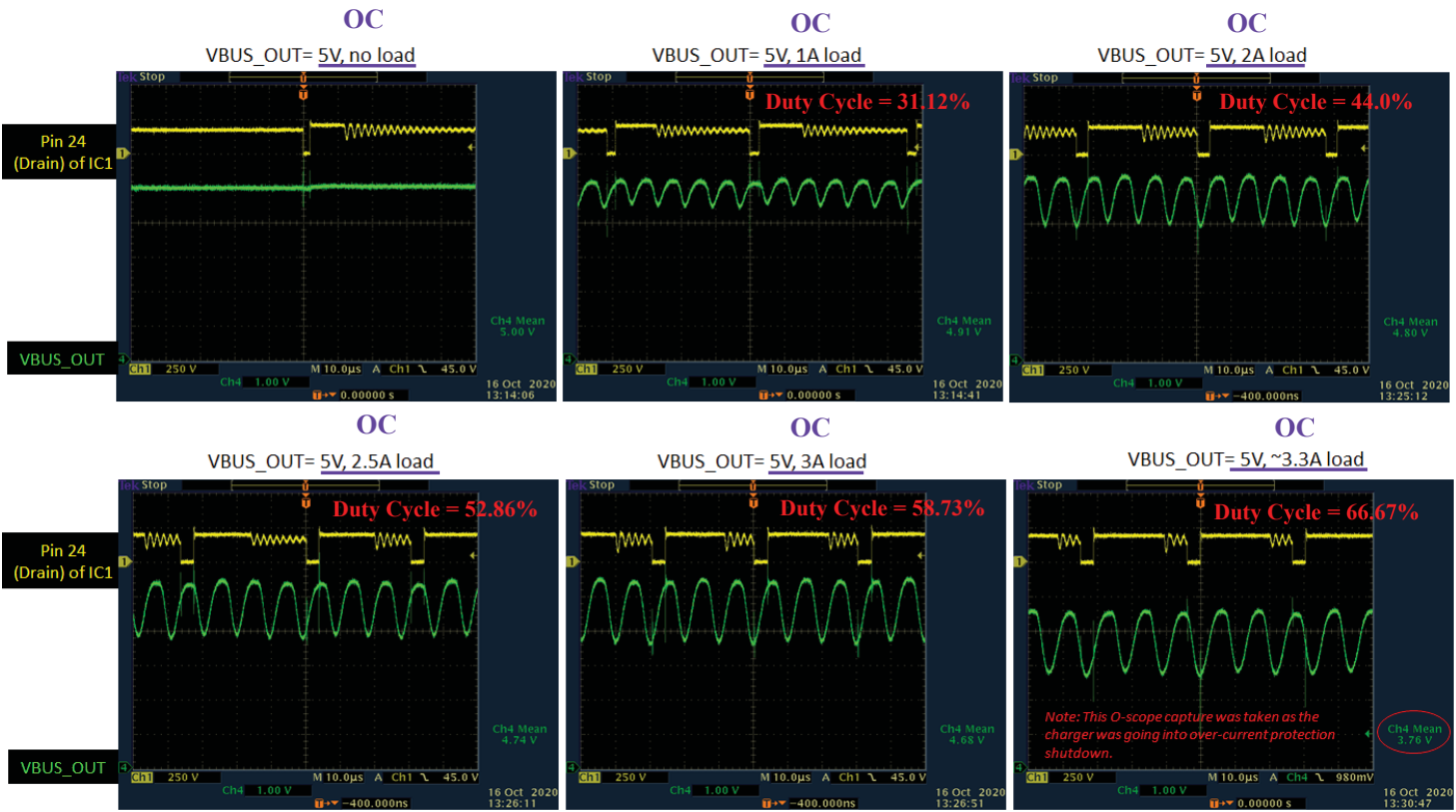| Claim 6	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845**

to provide a signal to control said **(DC) duty cycle** of said power switch as a function of said **(OC) output characteristic** and in accordance with said command,

OC

VBUS_OUT= 5V, no load

OC

VBUS_OUT= 5V, 1A load

Duty Cycle = 31.12%

OC

VBUS_OUT= 5V, 2A load

Duty Cycle = 44.0%

OC

VBUS_OUT= 5V, 2.5A load

Duty Cycle = 52.86%

OC

VBUS_OUT= 5V, 3A load

Duty Cycle = 58.73%

OC

VBUS_OUT= 5V, ~3.3A load

Duty Cycle = 66.67%

Note: This O-scope capture was taken as the charger was going into over-current protection shutdown.

Pin 24 (Drain) of IC1

VBUS_OUT

Claim 6	Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845

thereby regulating an **(IOC) internal operating characteristic** of said **(CON) power converter** to improve an operating efficiency thereof as a function of said **(OP) system operational state**.

CON

OP

IOC

Highly Integrated, Compact Footprint
- Multi-mode Quasi-Resonant (QR) / DCM / CCM flyback controller, high-voltage switch, secondary-side sensing and synchronous rectifier driver
- Optimized efficiency across line and load range
- Integrated FluxLink™, HIPOT-isolated, feedback link
- Instantaneous transient response
- Drives low-cost N-channel FET series load switch
- Integrated 3.6 V supply for external MCU

Source: InnoSwitch3-Pro Family, Rev. M 8/20, Note: The citation pertains to only the document excerpt not the schematics or other data.

Claim 6	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung EP-TA845**

thereby regulating an internal operating characteristic of said power converter to **(EFF) improve an operating efficiency** thereof as a function of said **(OP) system operational state**.

<div align="center">

OP   **EFF**

</div>

EP-TA845 (5v testing)

vin	I_in (A)	meas_W_in	V_out	I_out (A)	calc_W_out	meas_W_out	Efficiency
	0.008	0.000	5.040	0.000	0.000	0.000	
	0.011	0.346	5.040	0.020	0.101	0.146	0.422
	0.021	0.745	5.040	0.100	0.504	0.513	0.689
	0.063	2.886	5.010	0.500	2.505	2.554	0.885
	0.106	5.472	4.970	1.000	4.970	4.995	0.913
	0.165	8.330	4.920	1.500	7.380	7.432	0.892
	0.194	11.040	4.920	2.000	9.840	9.860	0.893
	0.233	13.760	4.850	2.500	12.125	12.290	0.893

EP-TA845 (9V testing)

vin	I_in (A)	meas_W_in	V_out	I_out (A)	calc_W_out	meas_W_out	Efficiency
	0.015	0.508	8.990	0.000	0.000	0.000	
	0.021	0.732	8.990	0.020	0.180	0.261	0.357
	0.036	1.415	8.970	0.100	0.897	0.916	0.647
	0.108	5.206	8.940	0.500	4.470	4.570	0.878
	0.193	9.804	8.910	1.000	8.910	9.030	0.921
	0.247	14.570	8.840	1.500	13.260	13.270	0.911
	0.314	19.410	8.820	2.000	17.640	17.640	0.909
	0.381	24.100	8.740	2.500	21.850	21.860	0.907
	0.441	28.730	8.710	3.000	26.130	26.110	0.909

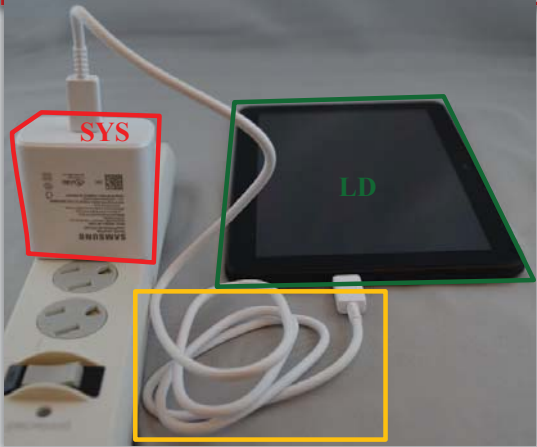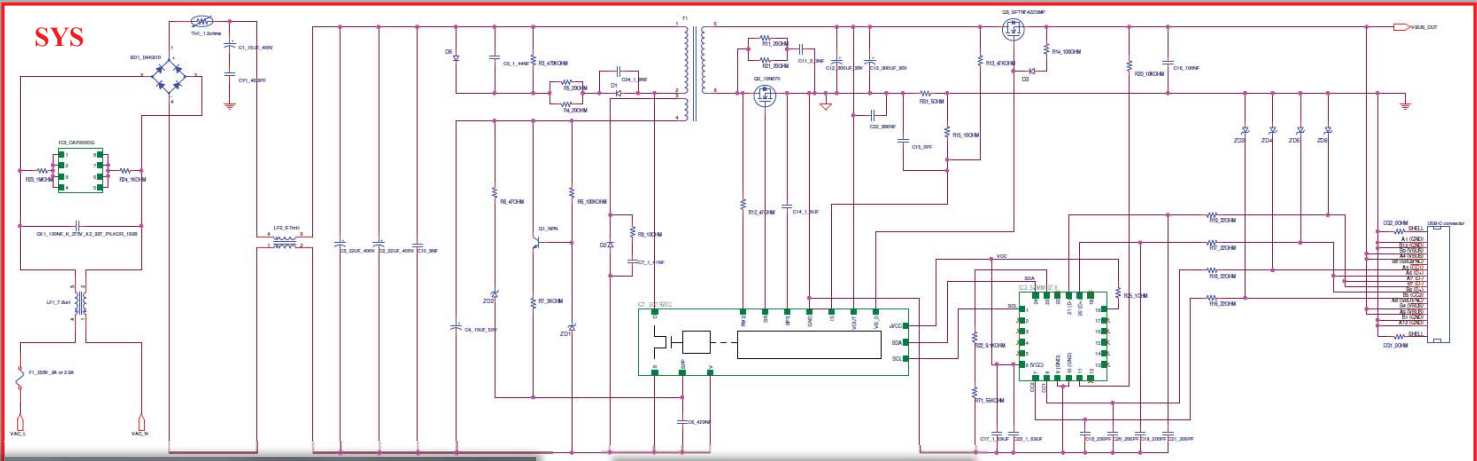Exhibit F - U.S. Patent No. 7,675,759 – Samsung S2MM101

Claim 16

A method of operating a **(SYS) power system** coupled to a **(LD) load**, comprising:

receiving a **(S) signal** indicating a **(OP) system operational state** of said **(LD) load**;

generating a **(PCOP) power converter operational state** as a function of said **(OP) system operational state**;

inducing a **(CON) power converter** to enter said **(PCOP) power converter operational state**; and

providing a **(OS) signal to control** a **(DC) duty cycle** of a **(PS) power switch** of said **(CON) power converter** as a function of an **(OC) output characteristic** thereof and in accordance with said **(PCOP) power converter operational state**,

thereby regulating an **(IOC) internal operating characteristic** of said **(CON) power converter** to improve an **(EFF) operating efficiency** thereof as a function of said **(OP) system operational state**.

Claim 16	Exhibit F - U.S. Patent No. 7,675,759 – Samsung S2MM101

A method of operating a **(SYS) power system** **coupled to** a **(LD) load**, comprising:

Claim 16	Exhibit F - U.S. Patent No. 7,675,759 – Samsung S2MM101

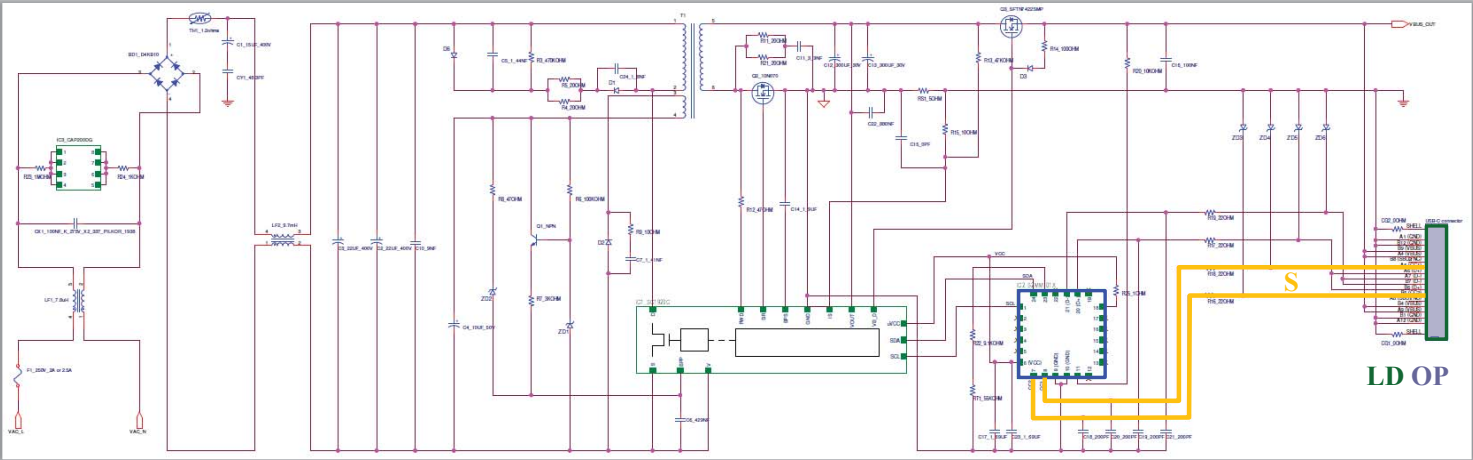receiving a **(S) signal** indicating a **(OP) system operational state** of said **(LD) load**;

LD OP

Table 3-5 USB Type-C Receptacle Interface Pin Assignments for USB 2.0-only Support

Pin	Signal Name	Description	Mating Sequence	Pin	Signal Name	Description	Mating Sequence
A1	GND	Ground return	First	B12	GND	Ground return	First
A2				B11			
A3				B10			
A4	Vbus	Bus Power	First	B9	Vbus	Bus Power	First
A5	CC1	Configuration Channel **S**	Second	B8	SBU2	Sideband Use (SBU)	Second
A6	Dp1	Positive half of the USB 2.0 differential pair – Position 1	Second	B7	Dn2	Negative half of the USB 2.0 differential pair – Position 2	Second
A7	Dn1	Negative half of the USB 2.0 differential pair – Position 1	Second	B6	Dp2	Positive half of the USB 2.0 differential pair – Position 2	Second
A8	SBU1	Sideband Use (SBU)	Second	B5	CC2	Configuration Channel **S**	Second
A9	Vbus	Bus Power	First	B4	Vbus	Bus Power	First
A10				B3			
A11				B2			
A12	GND	Ground return	First	B1	GND	Ground return	First

S

Table 4-10 Source Perspective

CC1	CC2	State	Position
Open	Open	Nothing attached	N/A
Rd	Open	Sink attached	①
Open	Rd		②
Open	Ra	Powered cable without Sink attached	①
Ra	Open		②
Rd	Ra	Powered cable with Sink, Vconn-Powered Accessory (VPA), or Vconn-Powered USB Device (VPD) attached	①
Ra	Rd		②
Rd	Rd	Debug Accessory Mode attached (Appendix B)	N/A
Ra	Ra	Audio Adapter Accessory Mode attached (Appendix A)	N/A

Highly Integrated, Compact Footprint   OP
- Multi-mode Quasi-Resonant (QR) / DCM / CCM flyback controller, high-voltage switch, secondary-side sensing and synchronous rectifier driver
- Optimized efficiency across line and load range

Source: InnoSwitch3-Pro Family, Rev. M 8/20, Universal Serial Bus Type-C Cable and Connector Specification, Release 2.0, August 2019
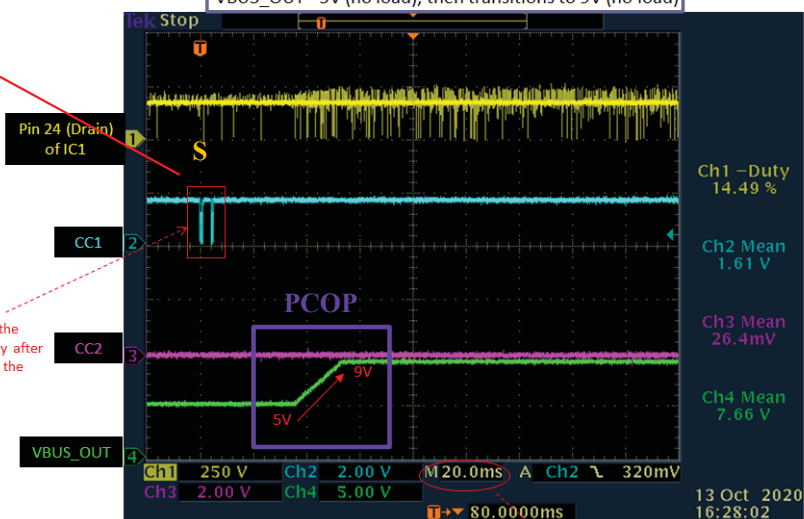
Claim 16	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung S2MM101**

generating a **(PCOP) power converter operational state** as a function of said **(OP) system operational state**;

Claim 16	Exhibit F - U.S. Patent No. 7,675,759 – Samsung S2MM101

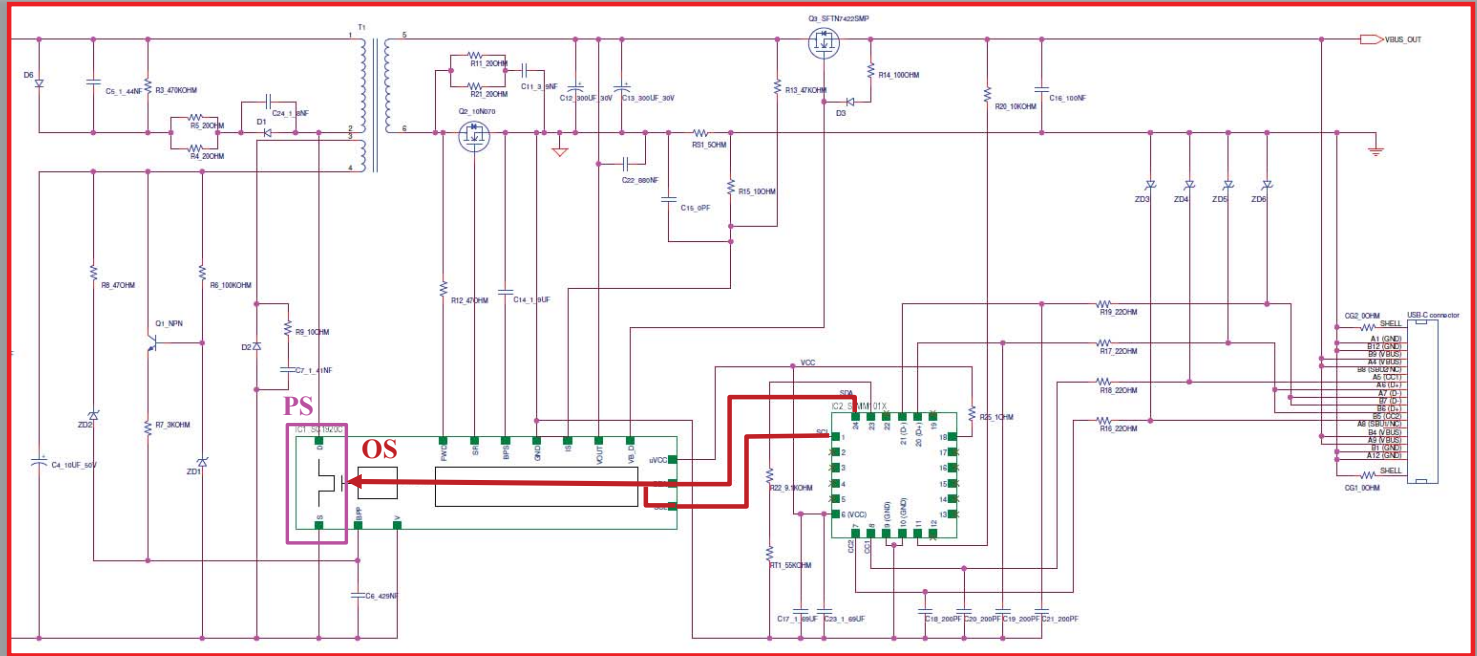inducing a **(CON) power converter** to enter said **(PCOP) power converter operational state**; and
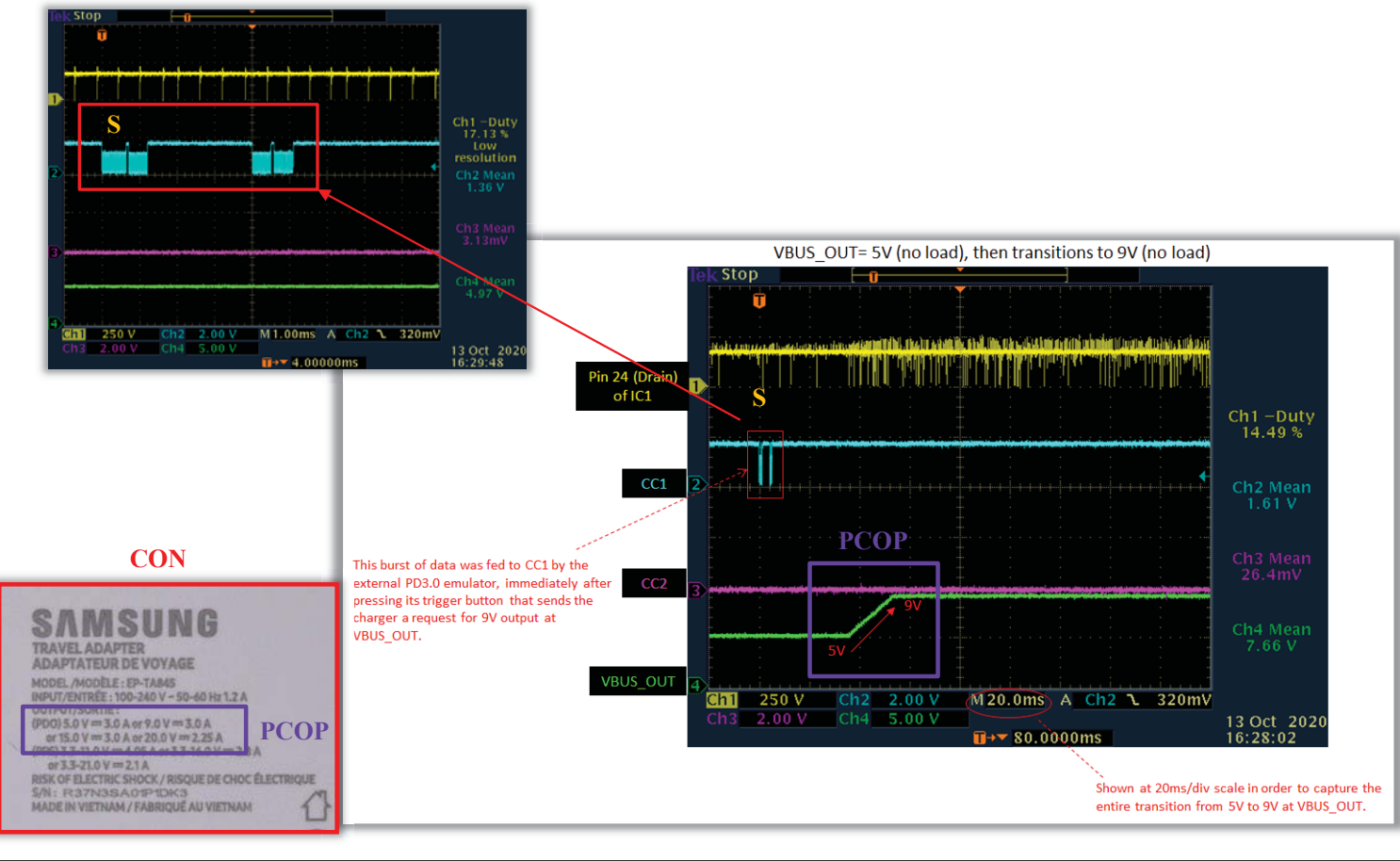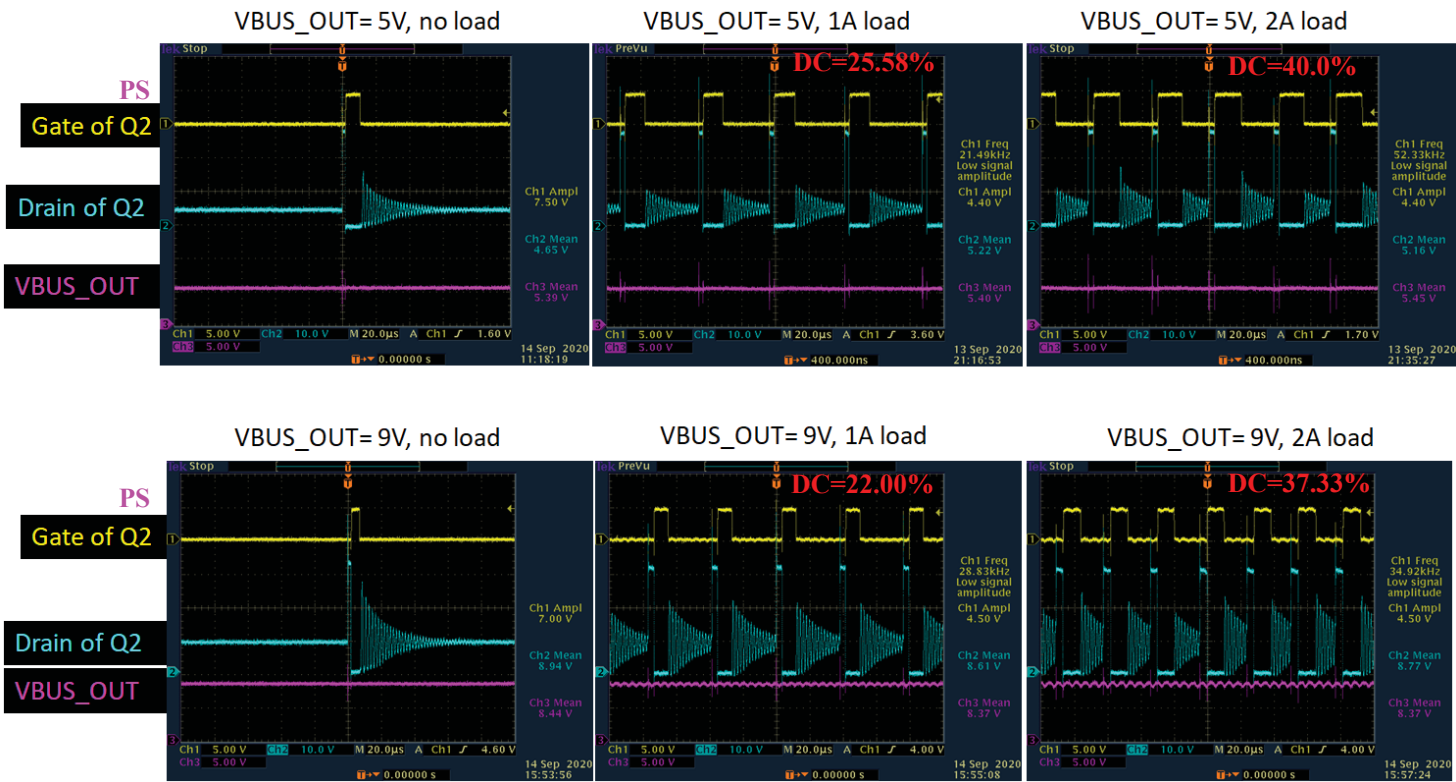
| Claim 16 | Exhibit F - U.S. Patent No. 7,675,759 – Samsung S2MM101 |

providing a **(OS) signal to control** a **(DC) duty cycle** of a **(PS) power switch** of said **(CON) power converter**

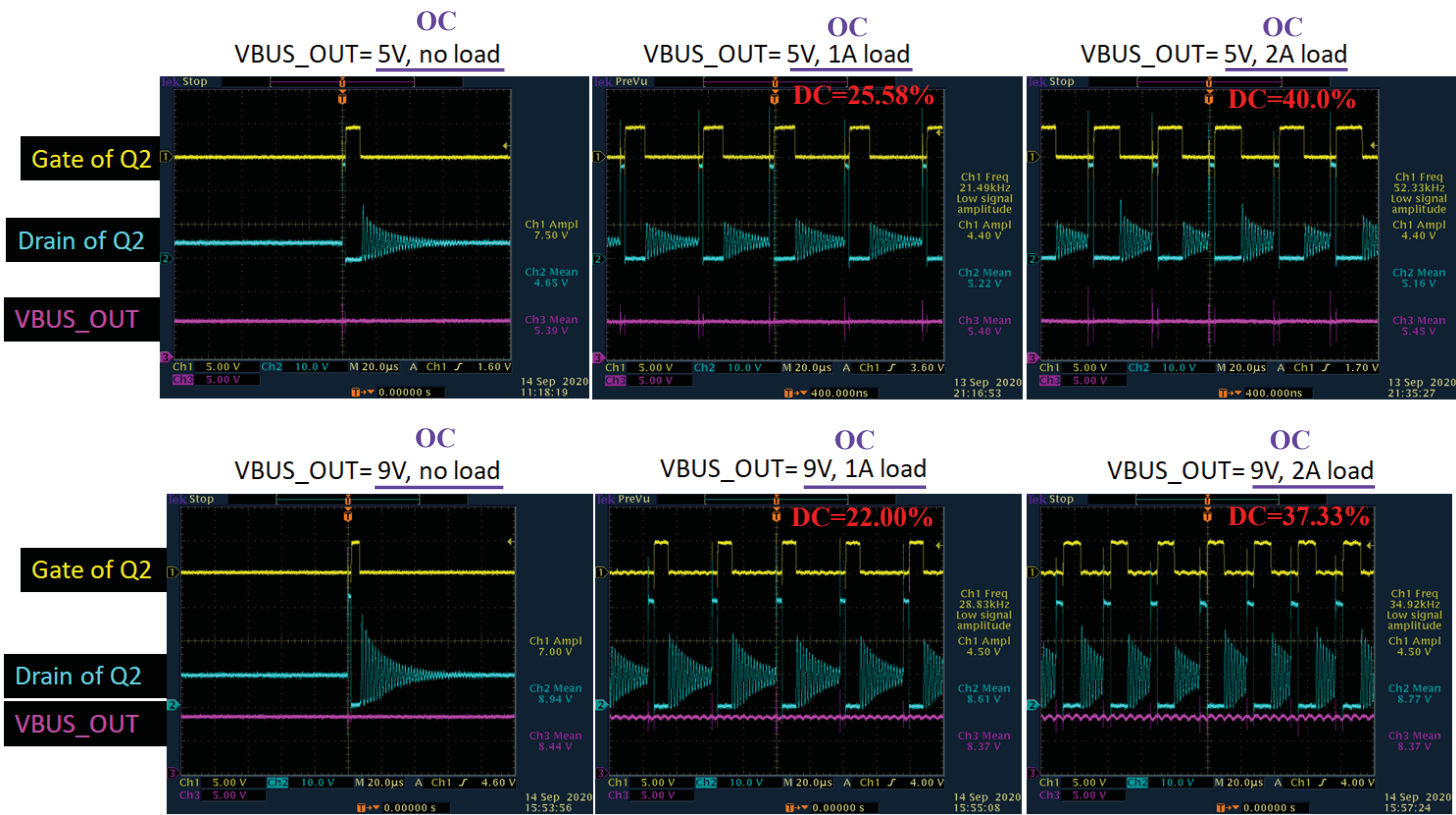| Claim 16	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung S2MM101**

providing a **(COM) signal** to control a **(DC) duty cycle** of a **(PS) power switch** of said **(CON) power converter**

<table>
<tr><td>Claim 16</td><td colspan="2" align="center">**Exhibit F - U.S. Patent No. 7,675,759 – Samsung S2MM101**</td></tr>
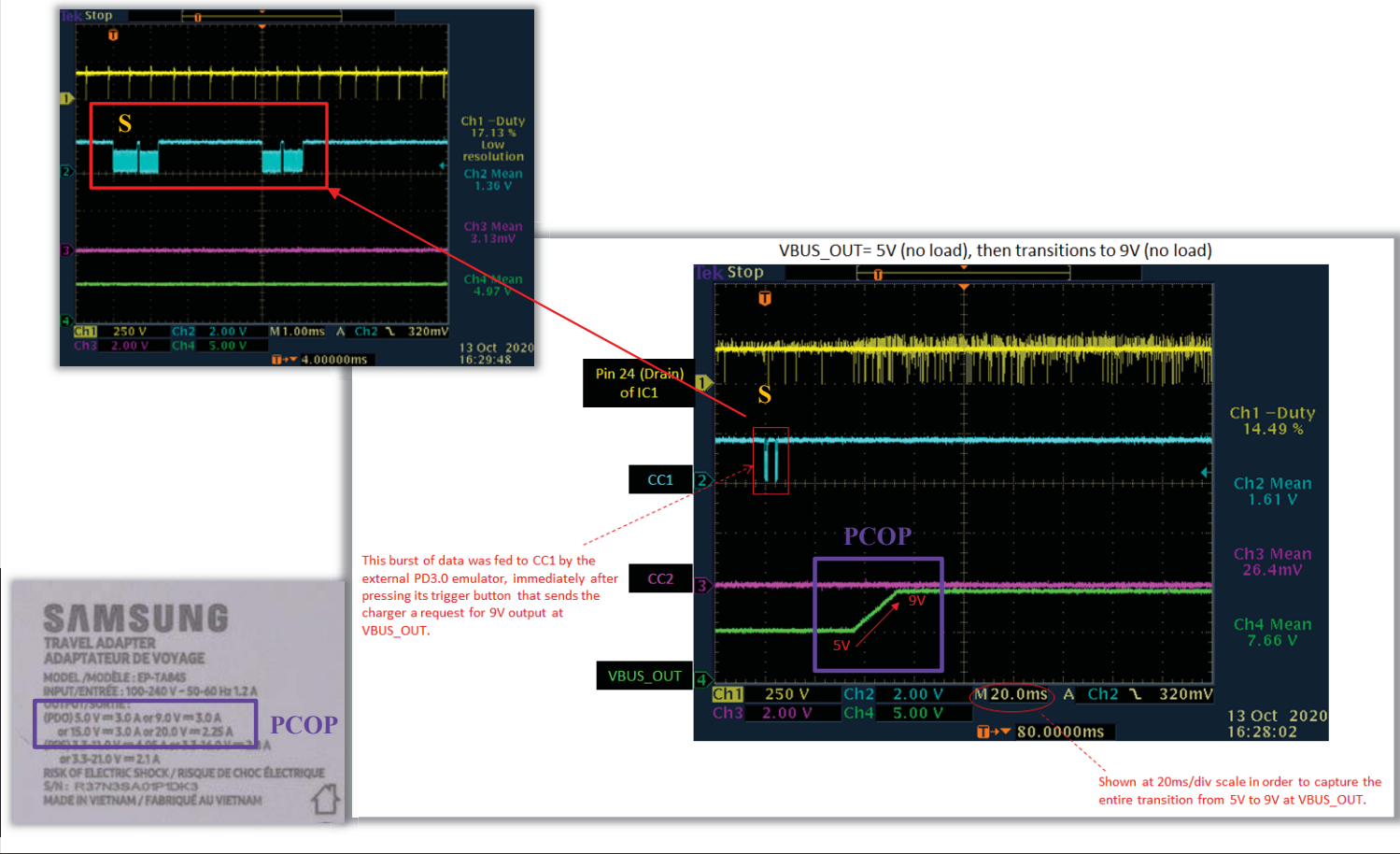</table>

as a function of an **(OC) output characteristic** thereof and in accordance with said **(PCOP) power converter operational state**,

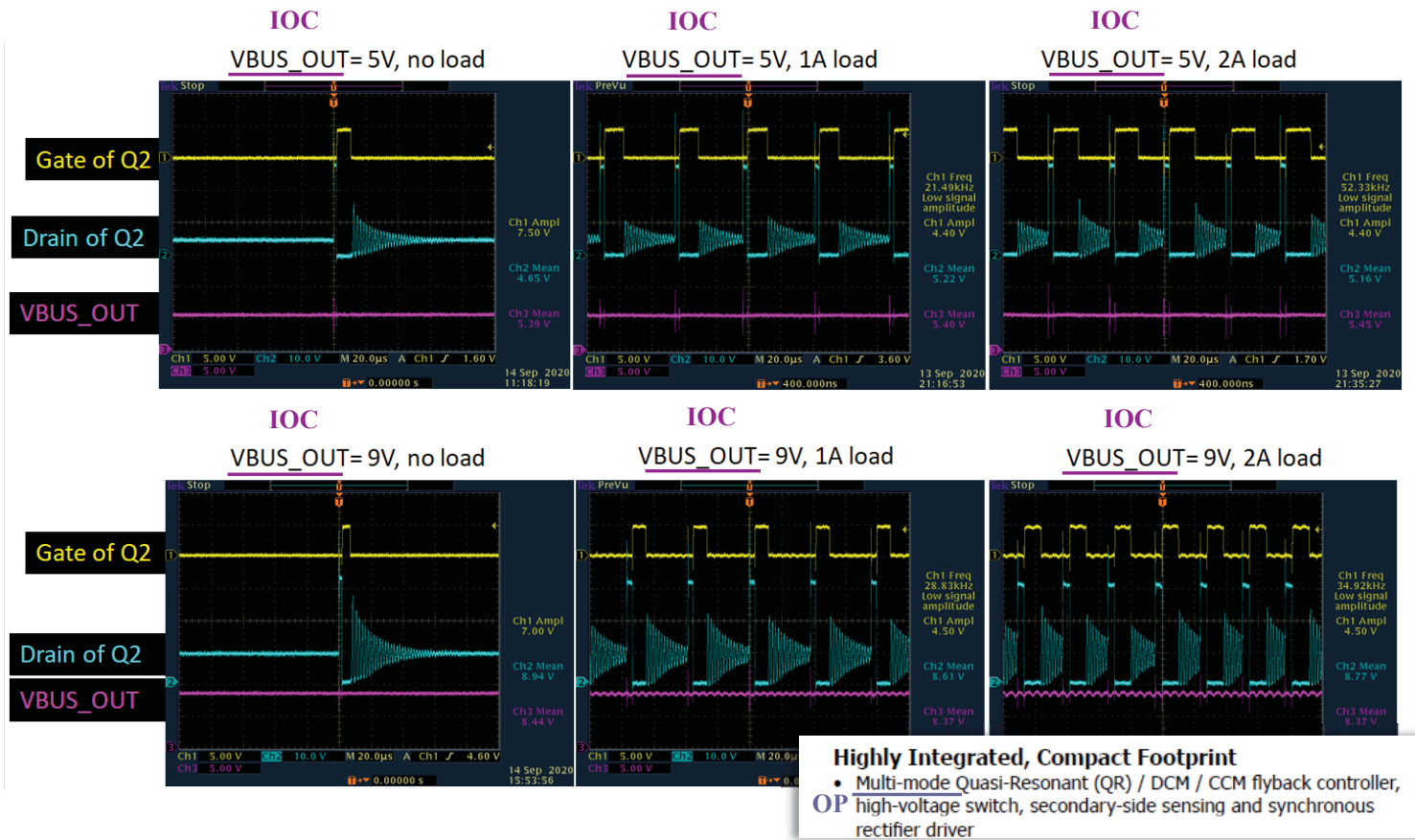| Claim 16 | Exhibit F - U.S. Patent No. 7,675,759 – Samsung S2MM101 |

as a function of an **(OC) output characteristic** thereof and in accordance with said **(PCOP) power converter operational state** ,

10

Claim 16	**Exhibit F - U.S. Patent No. 7,675,759 – Samsung S2MM101**

thereby regulating an **(IOC) internal operating characteristic** of said **(CON) power converter** to improve an **(EFF) operating efficiency** thereof as a function of said **(OP) system operational state**.
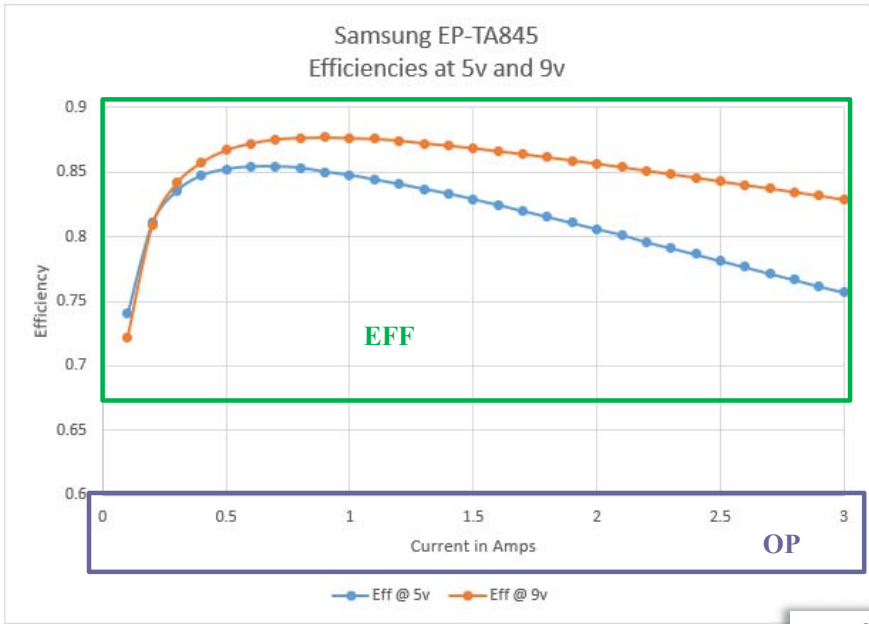

Source: InnoSwitch3-Pro Family, Rev. M 8/20, Note: The citation pertains to only the document excerpt not the schematics or other data.

Claim 16	Exhibit F - U.S. Patent No. 7,675,759 – Samsung S2MM101

thereby regulating an **(IOC) internal operating characteristic** of said **(CON) power converter** to improve an **(EFF) operating efficiency** thereof as a function of said **(OP) system operational state**.

Highly Integrated, Compact Footprint

OP

EFF
- Multi-mode Quasi-Resonant (QR) / DCM / CCM flyback controller, high-voltage switch, secondary-side sensing and synchronous rectifier driver
- Optimized efficiency across line and load range
- Integrated FluxLink™, HIPOT-isolated, feedback link
- Instantaneous transient response
- Drives low-cost N-channel FET series load switch
- Integrated 3.6 V supply for external MCU

Source: InnoSwitch3-Pro Family, Rev. M 8/20, Note: The citation pertains to only the document excerpt not the schematics or other data.